TOSHIBA TRANSISTOR SILICON NPN TRIPLE DIFFUSED MESA TYPE

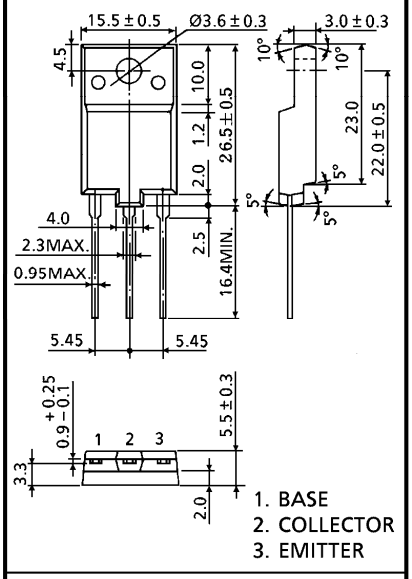
2SC5129

HORIZONTAL DEFLECTION OUTPUT FOR HIGH RESOLUTION DISPLAY, COLOR TV

HIGH SPEED SWITCHING APPLICATIONS

- High Speed : $t_f = 0.15\ \mu s$ (Typ.)
- High Voltage : $V_{CBO} = 1500$ V
- Low Saturation Voltage : $V_{CE\ (sat)} = 3$ V (Max.)
- Collector Metal (Fin) is Fully Covered with Mold Resin

Unit in mm



JEDEC	—
EIAJ	—
TOSHIBA	2-16E3A

Weight : 5.5 g (Typ.)

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Collector-Base Voltage		V_{CBO}	1500	V
Collector-Emitter Voltage		V_{CEO}	600	V
Emitter-Base Voltage		V_{EBO}	5	V
Collector Current	DC	I_C	10	A
	Pulse	I_{CP}	20	
Base Current		I_B	5	A
Collector Power Dissipation (Tc = 25°C)		P_C	50	W
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_{stg}	−55~150	°C

ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Collector Cut-off Current		I_{CBO}	$V_{CB} = 1500$ V, $I_E = 0$	—	—	1	mA
Emitter Cut-off Current		I_{EBO}	$V_{EB} = 5$ V, $I_C = 0$	—	—	10	μA
Emitter-Base Breakdown Voltage		$V_{(BR)\ CEO}$	$I_C = 10$ mA, $I_B = 0$	600	—	—	V
DC Current Gain		h_{FE} (1)	$V_{CE} = 5$ V, $I_C = 1$ A	10	—	30	—
		h_{FE} (2)	$V_{CE} = 5$ V, $I_C = 6$ A	4	—	8	
Collector-Emitter Saturation Voltage		$V_{CE\ (sat)}$	$I_C = 6$ A, $I_B = 1.5$ A	—	—	3	V
Base-Emitter Saturation Voltage		$V_{BE\ (sat)}$	$I_C = 6$ A, $I_B = 1.5$ A	—	1.0	1.4	V
Transition Frequency		f_T	$V_{CE} = 10$ V, $I_C = 0.1$ A	—	1.7	—	MHz
Collector Output Capacitance		Cob	$V_{CB} = 10$ V, $I_E = 0$, f = 1 MHz	—	135	—	pF
Switching Time (Fig.1)	Storage Time	t_{stg}	$I_{CP} = 5$ A, I_{B1} (end) = 1 A	—	2.5	4.0	μs
	Fall Time	t_f	$f_H = 64$ kHz	—	0.15	0.3	

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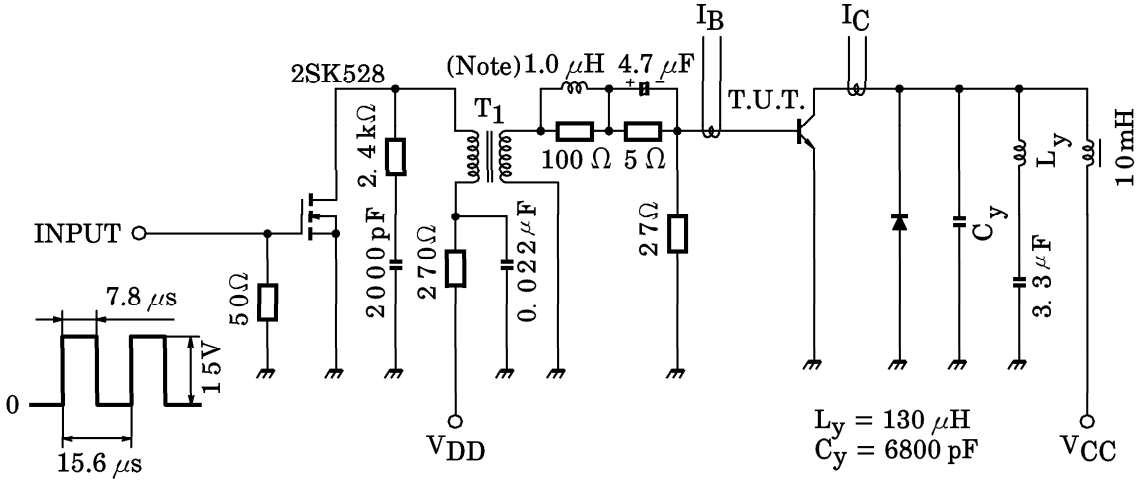
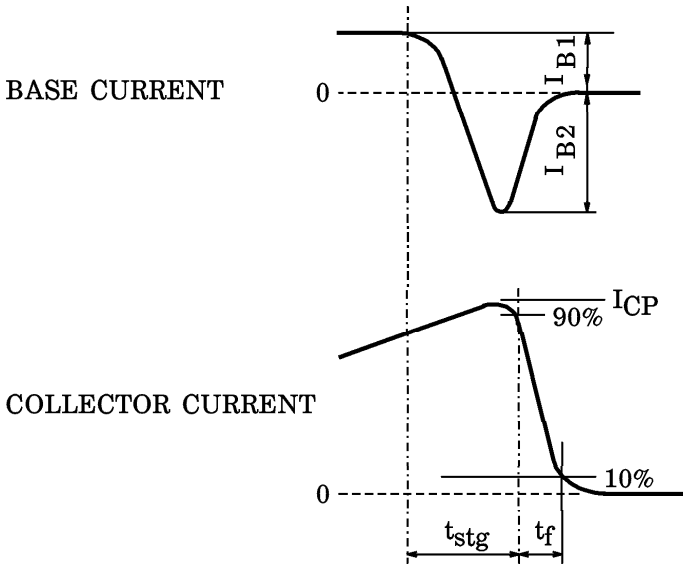
Fig.1 SWITCHING TIME TEST CIRCUIT (Inductive Load)



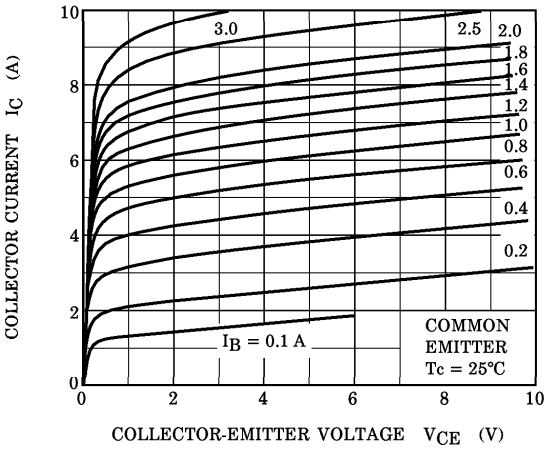
(Note) : Leakage Inductance of secondary winding LB is 1.2 μH.



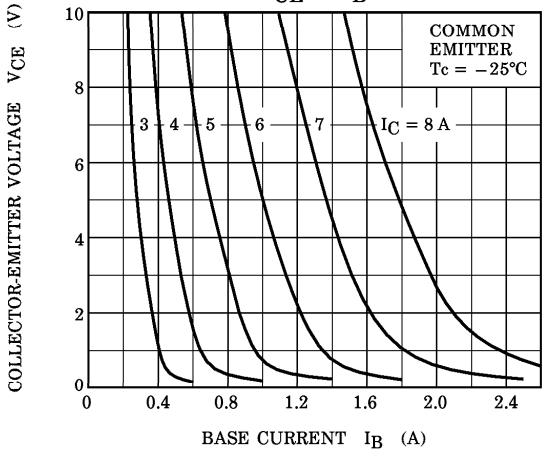
Base Current Gradient

$$dI_B / dt = \frac{I_{B1} + I_{B2}}{t_{stg}} (A / \mu s)$$

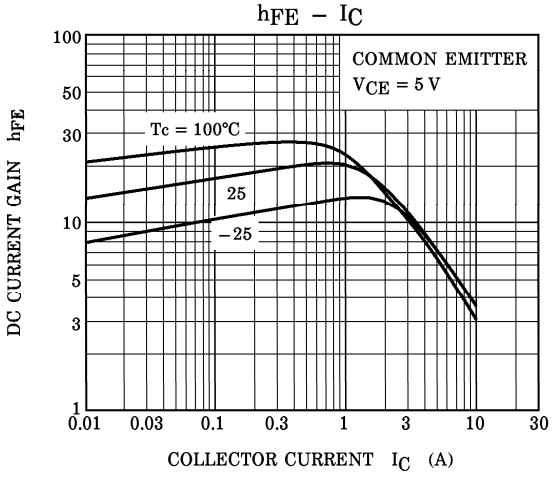
$I_C - V_{CE}$



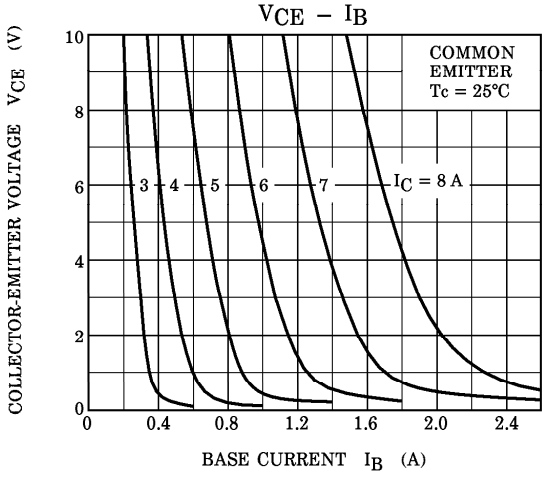
$V_{CE} - I_B$



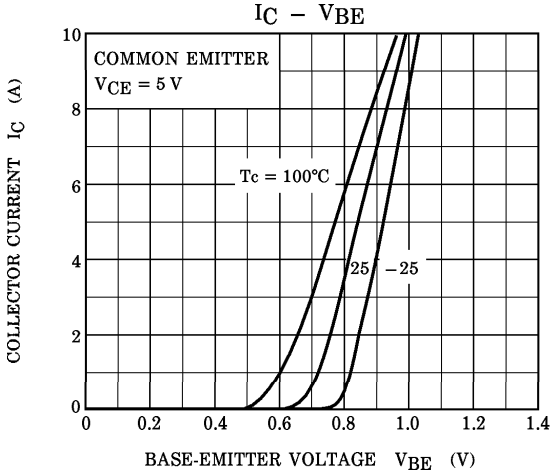
$h_{FE} - I_C$



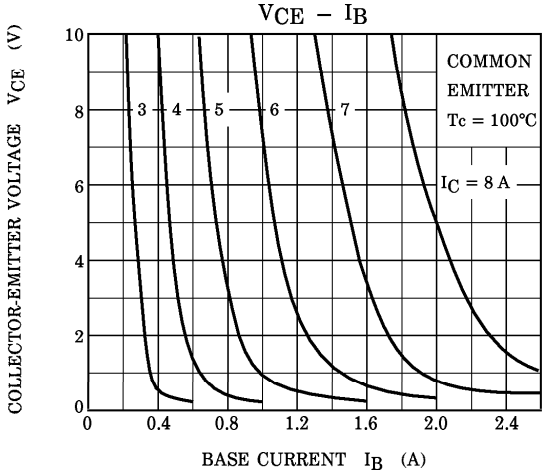
$V_{CE} - I_B$



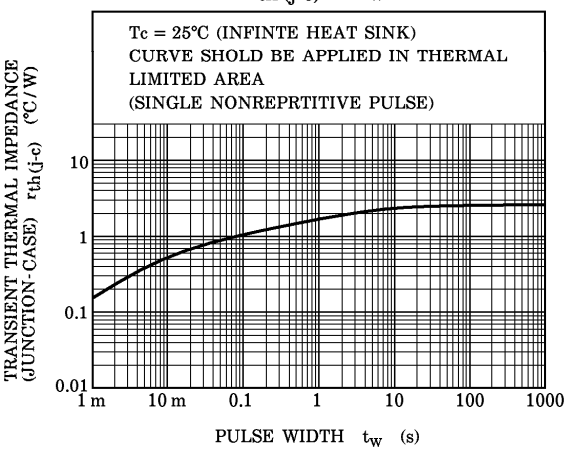
$I_C - V_{BE}$



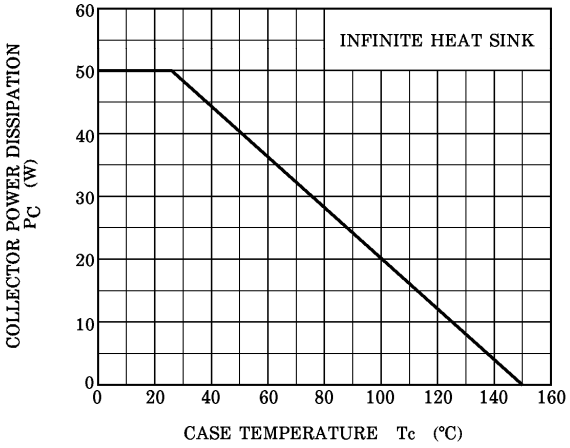
$V_{CE} - I_B$



$r_{th\,(j\text{-}c)}$ – t_w



P_C – Tc



SAFE OPERATING AREA