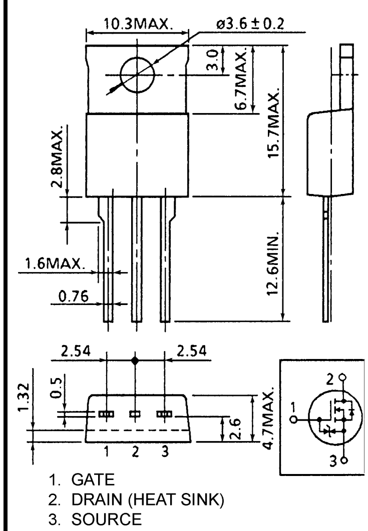
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (π−MOSV)

2SK2544

Switching Regulator Applications

- Low drain−source ON resistance : $R_{DS\ (ON)}$ = 0.9 Ω(typ.)
- High forward transfer admittance : $|Y_{fs}|$ = 5.5 S (typ.)
- Low leakage current : I_{DSS} = 100 μA (max) (V_{DS} = 600 V)
- Enhancement mode : V_{th} = 2.0~4.0 V (V_{DS} = 10 V, I_D = 1 mA)

Unit: mm



JEDEC	TO-220AB
JEITA	SC-46
TOSHIBA	2-10P1B

Weight: 2.0 g (typ.)

Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain−source voltage		V_{DSS}	600	V
Drain−gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	600	V
Gate−source voltage		V_{GSS}	±30	V
Drain current	DC (Note 1)	I_D	6	A
	Pulse (Note 1)	I_{DP}	24	A
Drain power dissipation (Tc = 25°C)		P_D	80	W
Single pulse avalanche energy (Note 2)		E_{AS}	345	mJ
Avalanche current		I_{AR}	6	A
Repetitive avalanche energy (Note 3)		E_{AR}	8	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55~150	°C

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th\ (ch-c)}$	1.56	°C / W
Thermal resistance, channel to ambient	$R_{th\ (ch-a)}$	83.3	°C / W

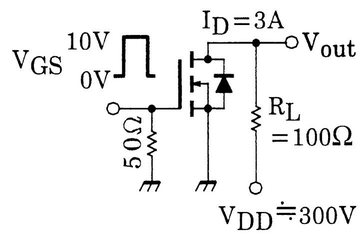
Note 1: Ensure that the channel temperature does not exceed 150°C..

Note 2: V_{DD} = 90 V, T_{ch} = 25°C (initial), L = 16.8 mH, R_G = 25 Ω, I_{AR} = 6 A

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

This transistor is an electrostatic-sensitive device.
Please handle with caution.

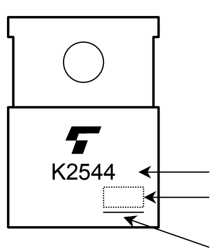
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±25 V, V_{DS} = 0 V	—	—	±10	μA
Gate−source breakdown voltage		$V_{(BR)\ GSS}$	I_G = ±10 μA, V_{GS} = 0 V	±30	—	—	V
Drain cut−off current		I_{DSS}	V_{DS} = 600 V, V_{DS} = 0 V	—	—	100	μA
Drain−source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	600	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	2.0	—	4.0	V
Drain−source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 10 V, I_D = 3 A	—	0.9	1.25	Ω
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 3 A	2.0	5.5	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	1300	—	pF
Reverse transfer capacitance		C_{rss}		—	130	—	
Output capacitance		C_{oss}		—	400	—	
Switching time	Rise time	t_r		—	25	—	ns
	Turn−on time	t_{on}		—	45	—	
	Fall time	t_f		—	40	—	
	Turn−off time	t_{off}	Duty ≦ 1%, t_w = 10μs	—	150	—	
Total gate charge (Gate−source plus gate−drain)		Q_g	V_{DD} ≈ 400 V, V_{GS} = 10 V, I_D = 6 A	—	30	—	nC
Gate−source charge		Q_{gs}		—	18	—	
Gate−drain (“miller”) charge		Q_{gd}		—	12	—	

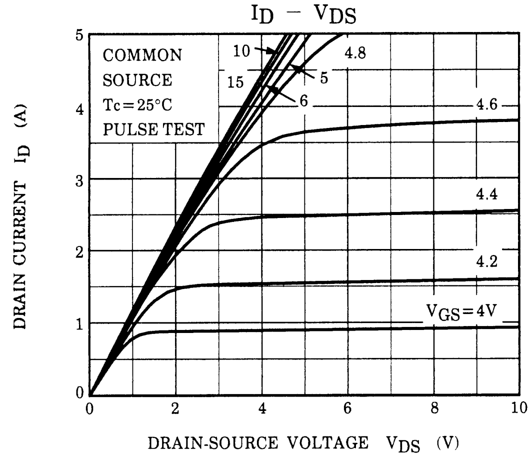
Source−Drain Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	6	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	24	A
Forward voltage (diode)	V_{DSF}	I_{DR} = 6 A, V_{GS} = 0 V	—	—	−1.7	V
Reverse recovery time	t_{rr}	I_{DR} = 6 A, V_{GS} = 0 V dI_{DR} / dt = 100 A / μs	—	1000	—	ns
Reverse recovery charge	Q_{rr}		—	7	—	μC

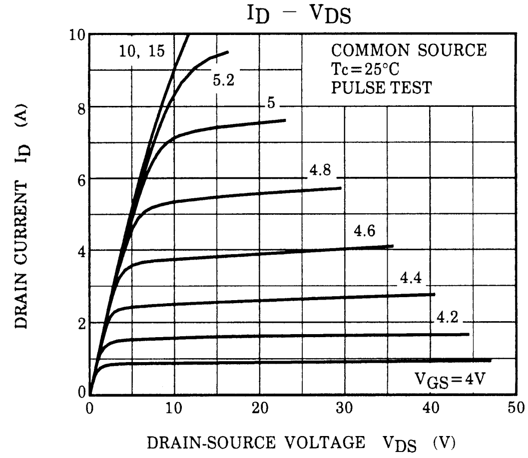
Marking



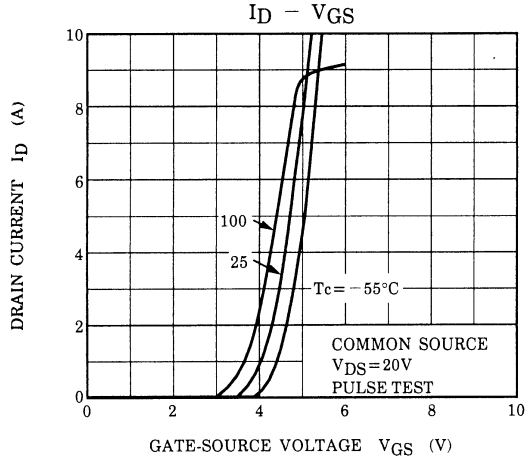
I_D – V_{DS}



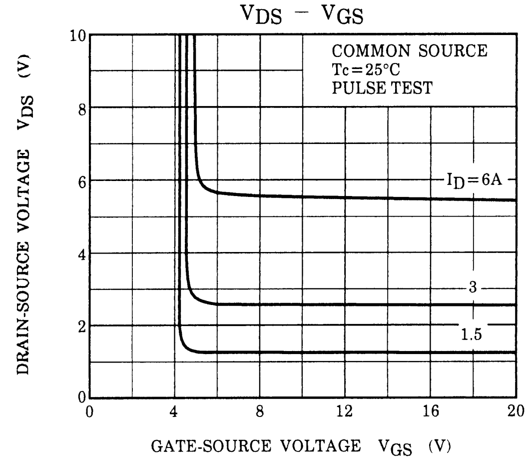
I_D – V_{DS}



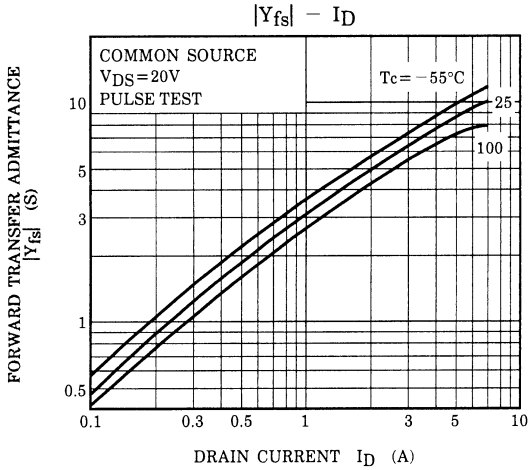
I_D – V_{GS}



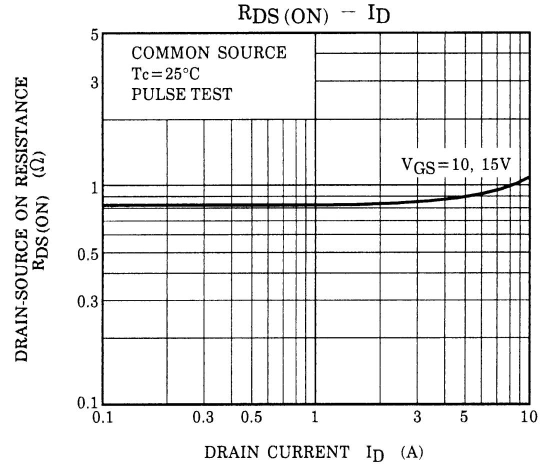
V_{DS} – V_{GS}

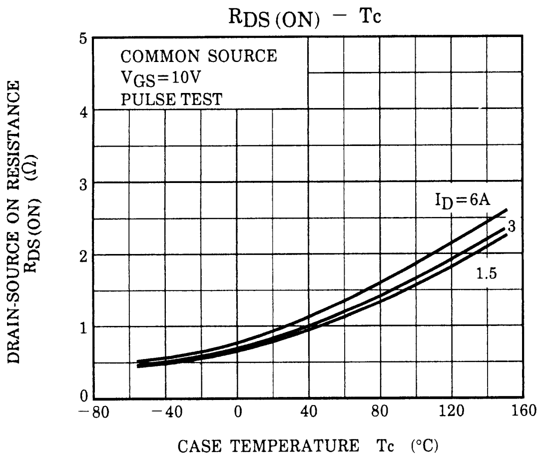


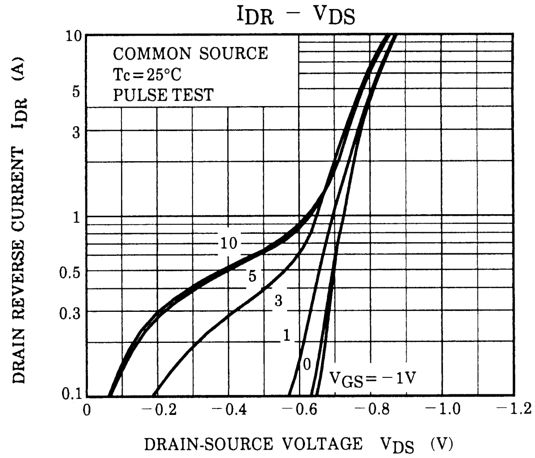
$|Y_{fs}|$ – I_D

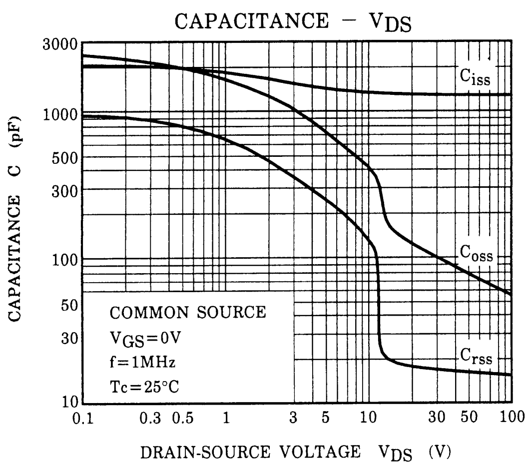


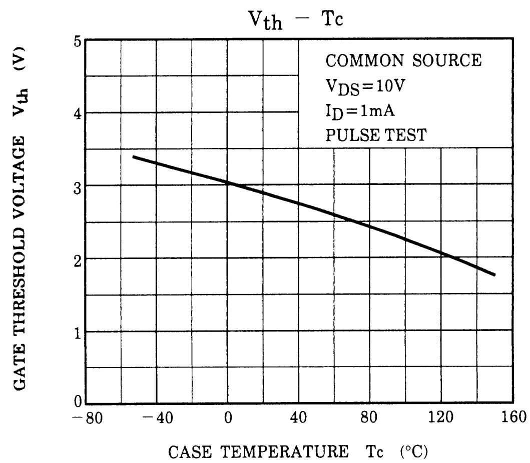
$R_{DS(ON)}$ – I_D

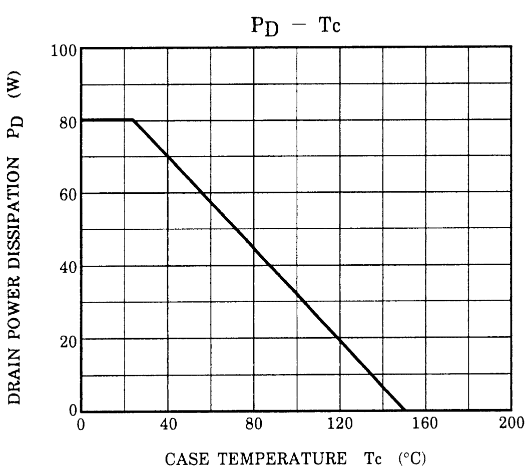


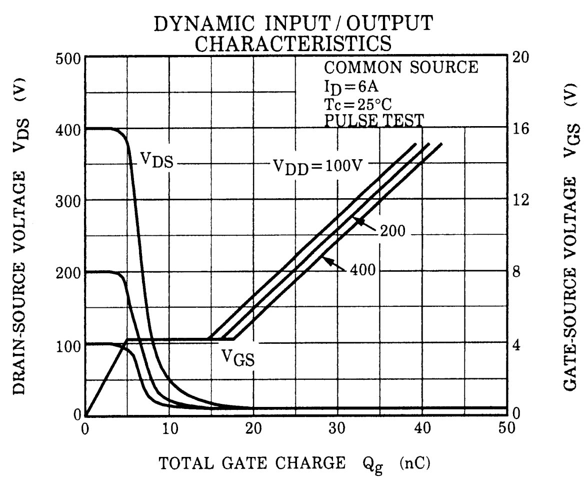

RDS (ON) − Tc
COMMON SOURCE
VGS = 10V
PULSE TEST
ID = 6A
3
1.5
DRAIN-SOURCE ON RESISTANCE RDS (ON) (Ω)
CASE TEMPERATURE Tc (°C)


IDR − VDS
COMMON SOURCE
Tc = 25°C
PULSE TEST
10
5
3
1
0
VGS = −1V
DRAIN REVERSE CURRENT IDR (A)
DRAIN-SOURCE VOLTAGE VDS (V)

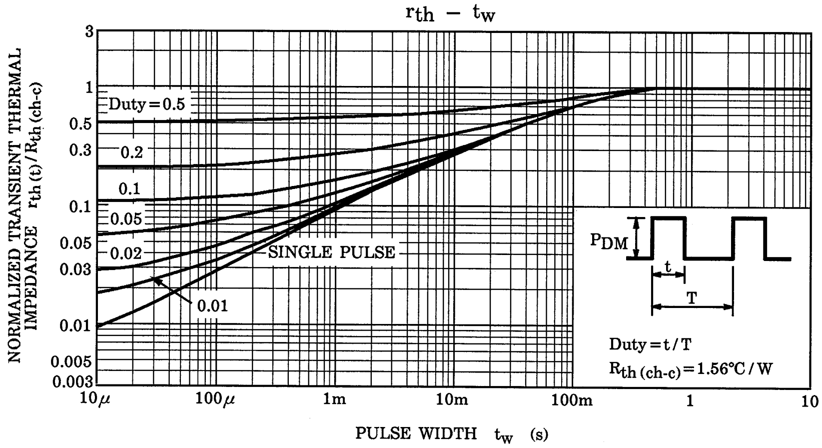

CAPACITANCE − VDS
Ciss
Coss
Crss
COMMON SOURCE
VGS = 0V
f = 1MHz
Tc = 25°C
CAPACITANCE C (pF)
DRAIN-SOURCE VOLTAGE VDS (V)


Vth − Tc
COMMON SOURCE
VDS = 10V
ID = 1mA
PULSE TEST
GATE THRESHOLD VOLTAGE Vth (V)
CASE TEMPERATURE Tc (°C)

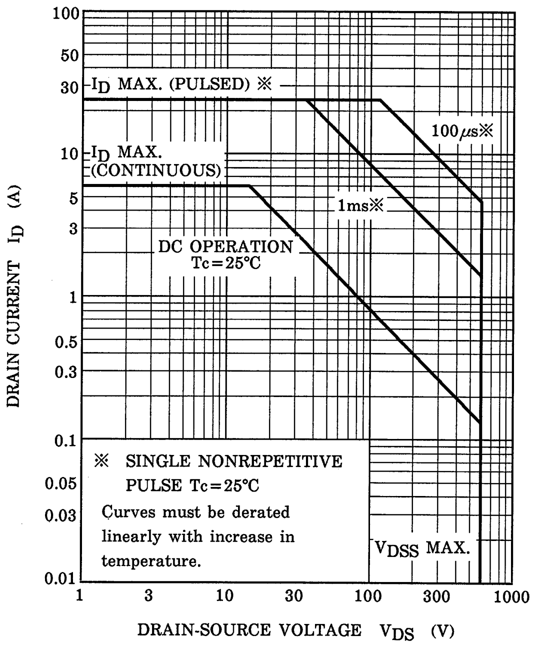

PD − Tc
DRAIN POWER DISSIPATION PD (W)
CASE TEMPERATURE Tc (°C)


DYNAMIC INPUT / OUTPUT CHARACTERISTICS
COMMON SOURCE
ID = 6A
Tc = 25°C
PULSE TEST
VDS
VDD = 100V
200
400
VGS
DRAIN-SOURCE VOLTAGE VDS (V)
GATE-SOURCE VOLTAGE VGS (V)
TOTAL GATE CHARGE Qg (nC)

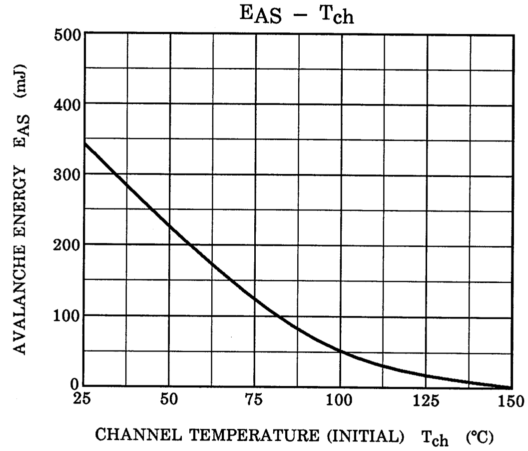
r_{th} – t_w

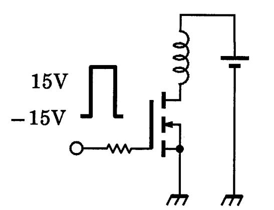


SAFE OPERATING AREA

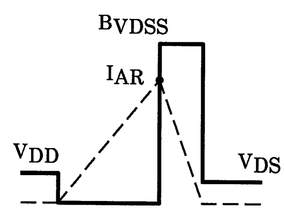


E_{AS} – T_{ch}





TEST CIRCUIT



WAVE FORM

R_G = 25 Ω
V_{DD} = 90 V, L = 16.8 mH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

RESTRICTIONS ON PRODUCT USE