

BA3520 BA3520F

3 V dual pre- and power amplifier

The BA3520 and BA3520F ICs are dual channel preamplifier and power amplifiers that contain all basic signal circuits necessary for a tape player.

The preamplifiers are direct coupled and the power amplifiers have a built-in fixed-gain NF circuit, making an output coupling capacitor unnecessary.

Features

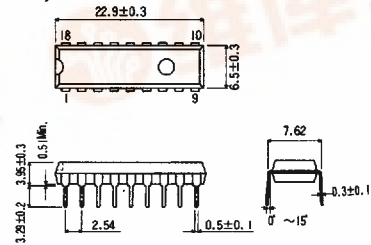
- available in DIP18 and SOP18 packages
- low voltage operation (1.8 ~ 4.0 Vdc)
- preamplifier has high voltage gain (78 dB), low noise (1.1 μV_{rms}) and low distortion (0.03%)
- power amplifier has high output (30 mW \times 2), low noise (50 μV_{rms}) and low distortion (0.5%)
- has a built in EVR. A-curve characteristics for EVR obtained are from the VR of the B-curve
- no oscillation protector required for power amplifier
- built in muting circuit

Applications

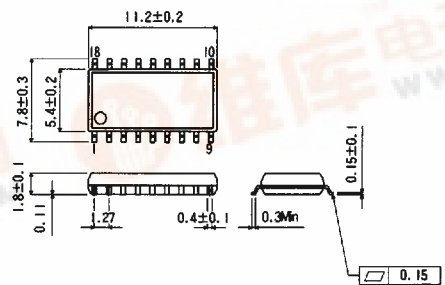
- 3 V tape player
- 3 V radio cassette player

Dimensions (Units : mm)

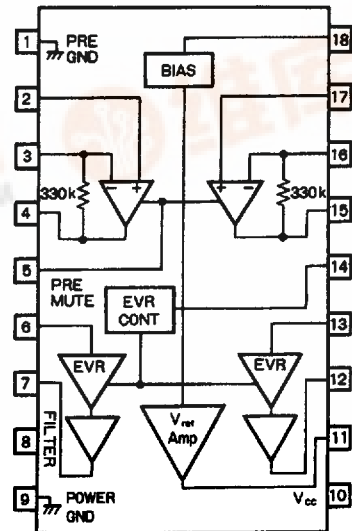
BA3520 (DIP18)



BA3520F (SOP18)



Block diagram



Absolute maximum ratings ($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Limits	Unit	Conditions
Power supply voltage	V_{CC}	6.0	V	
Power dissipation	BA3520	1000	mW	Reduce power by 10 mW for each degree above 25°C .
	BA3520F	550		Reduce power by 5.5 mW for each degree above 25°C . Mounted on a $50 \times 50 \times 1.6$ mm glass epoxy PCB.
Operating temperature	T_{opr}	$-25 \sim +75$	$^\circ\text{C}$	
Storage temperature	T_{stg}	$-55 \sim +125$	$^\circ\text{C}$	

Recommended operating conditions ($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Power supply voltage	V_{CC}	1.8	3.0	4.0	V	

**Electrical characteristics (unless otherwise noted, $T_a = 25^\circ\text{C}$, $V_{CC} = 3$ V, $f = 1$ kHz)
(Sheet 1 of 2)**

Parameter	Symbol	Min	Typical	Max	Unit	Conditions
Quiescent current	I_Q	10	15	20	mA	$V_{IN} = 0$ V _{rms}
Channel separation	CS	30	40		dB	$R_G = 2.2$ k Ω , $R_L = 32$ Ω

Preamplifier ($R_L = R_{IN}$ (EVR))

Open loop voltage gain	G_{VO}	72	78		dB	$V_O = 200$ mV _{rms}
Closed loop voltage gain	G_{VC1}	28	31	34	dB	$V_O = 100$ mV _{rms}
Output voltage	V_{OM}	300	500		mV _{rms}	THD = 1%
Total harmonic distortion	THD ₁		0.03	0.15	%	$V_O = 0.2$ V _{rms}
Input bias current	I_{B1}		100	300	nA	$V_{IN} = 0$ V _{rms}
Input conversion noise voltage	V_{NIN}		1.1	1.8	μV_{rms}	$R_g = 2.2$ k Ω , BPF = 20 Hz ~ 20 kHz
Ripple rejection	RR ₁	59	65		dB	$V_{RR} = -20$ dBV, $f_{RR} = 100$ Hz

Power amplifier ($R_L = 32\Omega$) (except P_{OUT1})

Rated output 1	P_{OUT1}	25	30		mW/ch	$R_L = 16$ Ω , THD = 10%
Rated output 2	P_{OUT2}	15	18		mW/ch	$R_L = 32$ Ω , THD = 10%
Closed loop voltage gain	G_{VC2}	33	36	39	dB	$V_O = 300$ mV _{rms}
Total harmonic distortion	THD ₂		0.5	1.5	%	EVR = max, $P_O = 5$ mW
Output noise voltage	V_{NO}		50	80	μV_{rms}	EVR = min, BPF = 20 Hz ~ 20 kHz

BA3520, BA3520F Pre- and power amplifiers for headphone stereos

Electrical characteristics (unless otherwise noted, $T_a = 25^\circ\text{C}$, $V_{CC} = 3\text{ V}$, $f = 1\text{ kHz}$)
(Sheet 2 of 2)

Parameter	Symbol	Min	Typical	Max	Unit	Conditions
Ripple rejection	RR_2	60	65		dB	$V_{RR} = -20\text{ dBV}$, $f_{RR} = 100\text{ Hz}$,
EVR input resistance	R_{IN}	21	30	39	$k\Omega$	
EVR attenuation ratio	ATT	70	80		dB	0 dB = -10 dBV, EVR = max When EVR = max, set the input so power amp output $V_0 = -10\text{ dBV}$. Measure the attenuation of V when EVR = min in that state.

Figure 1 Test circuit

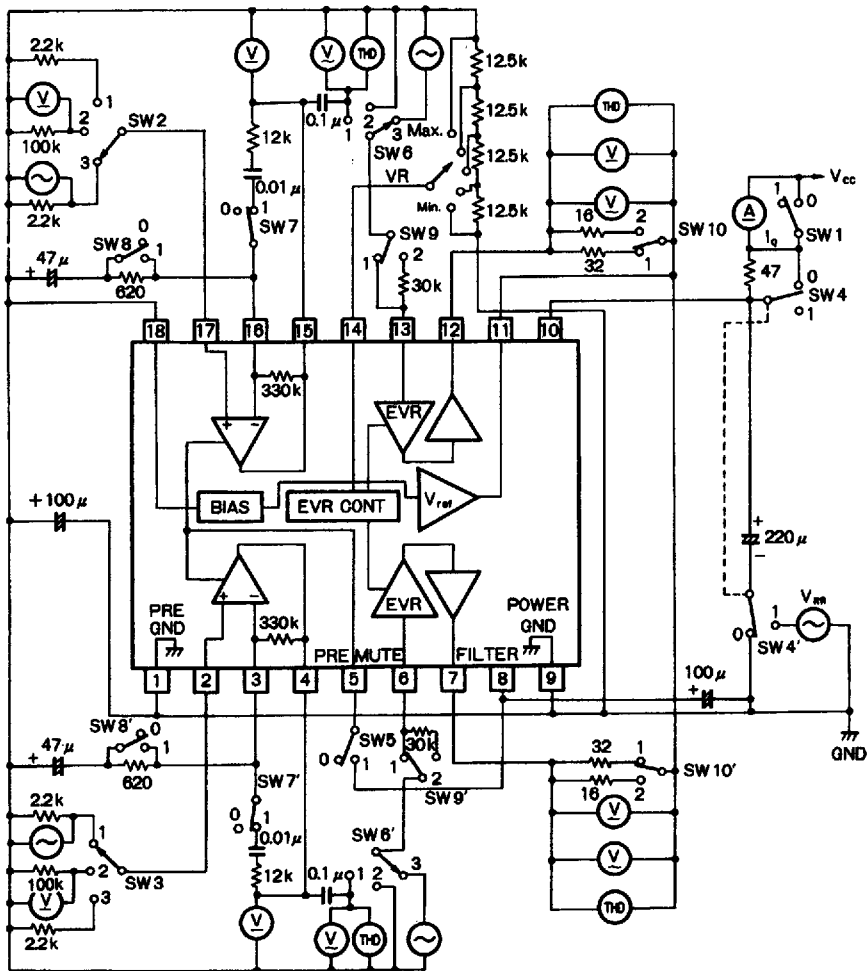
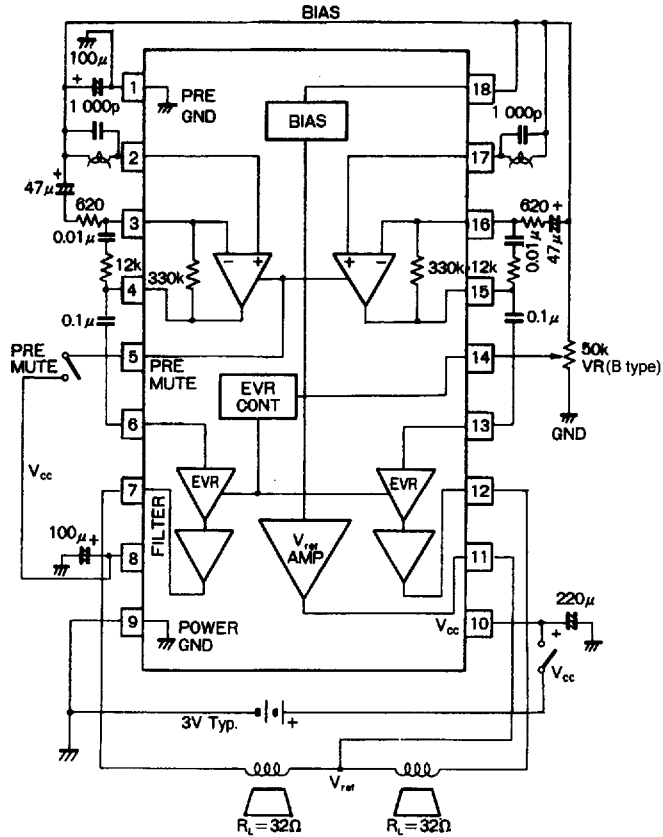


Figure 2 Application example



Gain and the dynamic range with EVR IN

Figure 3 EVR equivalent circuit diagram

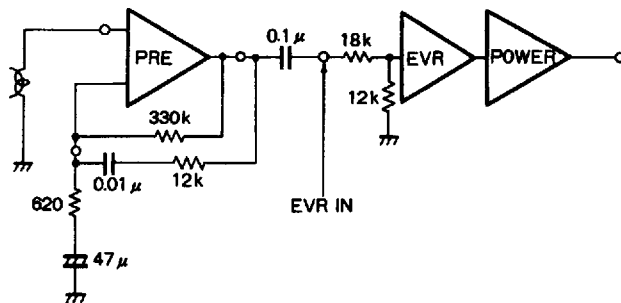
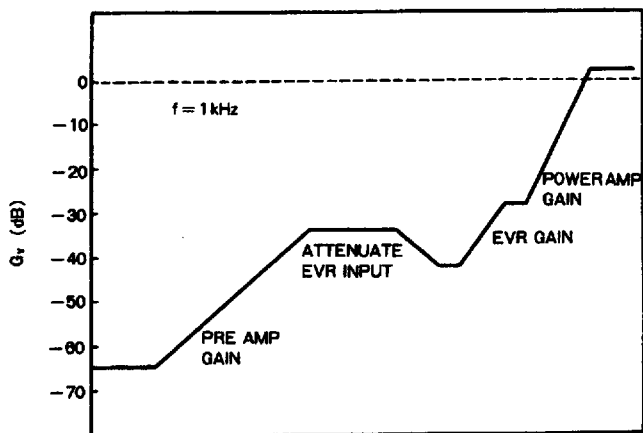


Figure 4 Gain distribution



The total harmonic distortion for the input dynamic range is a minimum for $V_{IN} = -30.4 \text{ dBV}$ as shown in Figure 7. A gain distribution for the application example is shown in Figure 4.

Note: When connecting to a graphic equalizer it is necessary to set the signal level so that it does not exceed the limitations to the EVR IN.

Electrical characteristic curves

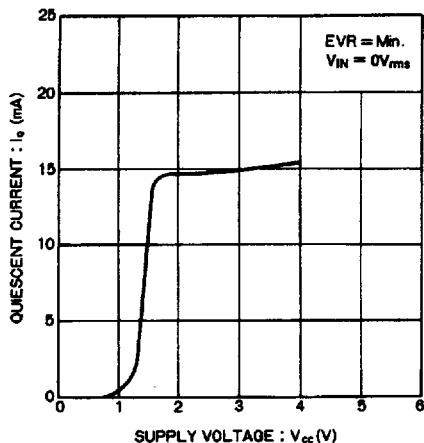


Figure 5

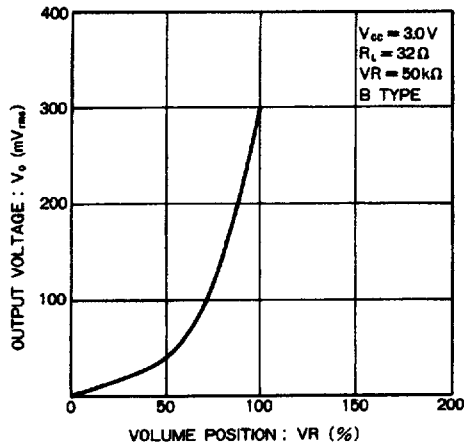


Figure 6

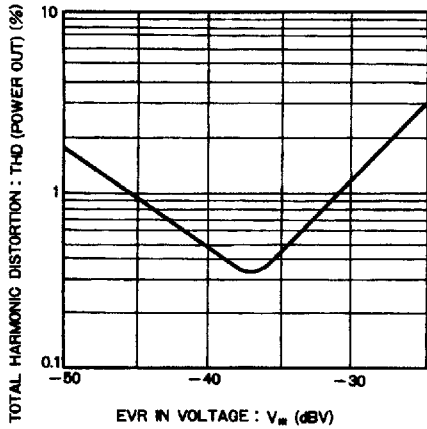


Figure 7

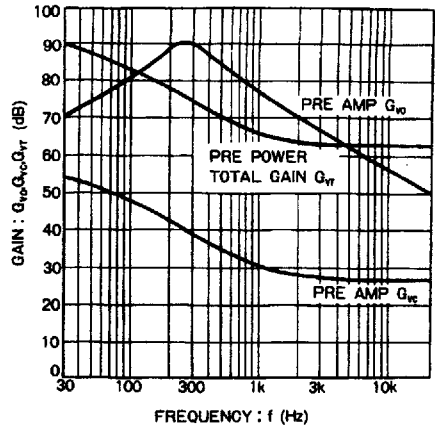


Figure 8

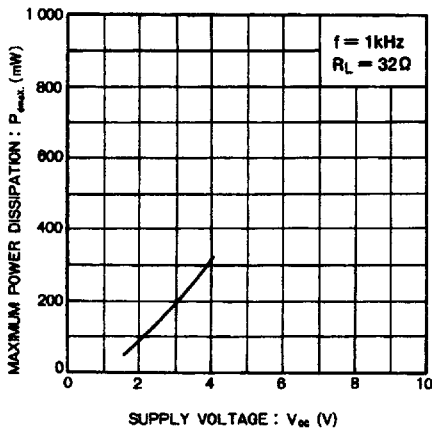


Figure 9

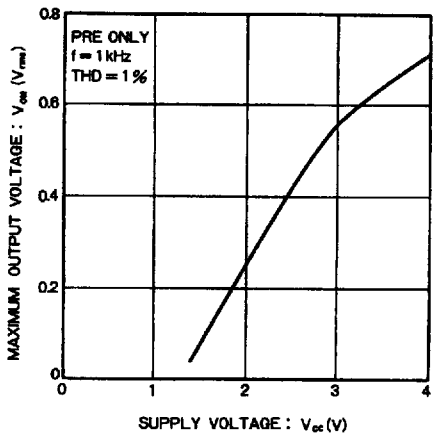


Figure 10

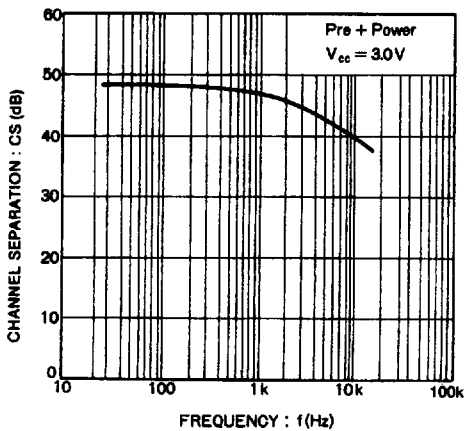


Figure 11

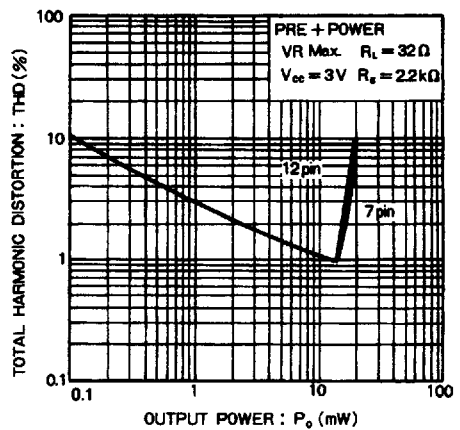


Figure 12