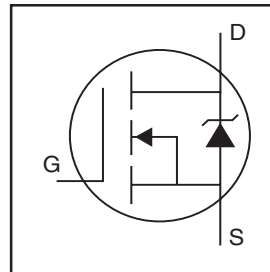


Features

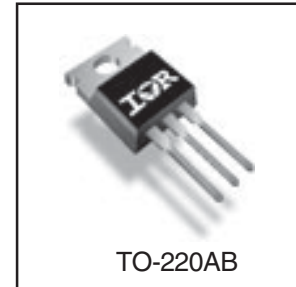
- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax



$V_{DSS} = 40V$
$R_{DS(on)} = 2.3m\Omega$
$I_D = 75A$

Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon limited)	280	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (See Fig.9)	200	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Package limited)	75	
I_{DM}	Pulsed Drain Current ①	1080	
$P_D @ T_C = 25^\circ C$	Power Dissipation	330	W
	Linear Derating Factor	2.2	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	670	mJ
E_{AS} (tested)	Single Pulse Avalanche Energy Tested Value②	1160	
I_{AR}	Avalanche Current③	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy③		mJ
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

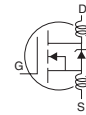
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.45	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	40	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.031	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	1.8	2.3	mΩ	V _{GS} = 10V, I _D = 75A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = 10V, I _D = 250μA
g _{fs}	Forward Transconductance	130	—	—	S	V _{DS} = 10V, I _D = 75A
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 40V, V _{GS} = 0V
		—	—	250		V _{DS} = 40V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V _{GS} = -20V
Q _g	Total Gate Charge	—	160	240	nC	I _D = 75A
Q _{gs}	Gate-to-Source Charge	—	41	62		V _{DS} = 32V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	66	99		V _{GS} = 10V ④
t _{d(on)}	Turn-On Delay Time	—	13	—	ns	V _{DD} = 20V
t _r	Rise Time	—	120	—		I _D = 75A
t _{d(off)}	Turn-Off Delay Time	—	130	—		R _G = 2.5Ω
t _f	Fall Time	—	130	—		V _{GS} = 10V ④
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	7.5	—		
C _{ISS}	Input Capacitance	—	6450	—	pF	V _{GS} = 0V
C _{OSS}	Output Capacitance	—	1690	—		V _{DS} = 25V
C _{RSS}	Reverse Transfer Capacitance	—	840	—		f = 1.0MHz, See Fig. 5
C _{OSS}	Output Capacitance	—	5350	—		V _{GS} = 0V, V _{DS} = 1.0V, f = 1.0MHz
C _{OSS}	Output Capacitance	—	1520	—		V _{GS} = 0V, V _{DS} = 32V, f = 1.0MHz
C _{OSS eff.}	Effective Output Capacitance ⑤	—	2210	—		V _{GS} = 0V, V _{DS} = 0V to 32V



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	280	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	1080		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 75A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	56	84	ns	T _J = 25°C, I _F = 75A, V _{DD} = 20V
Q _{rr}	Reverse Recovery Charge	—	67	100	nC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Limited by T_{Jmax}; starting T_J = 25°C, L=0.24mH, R_G = 25Ω, I_{AS} = 75A, V_{GS} = 10V. Part not recommended for use above this value.
- ③ I_{SD} ≤ 75A, di/dt ≤ 220A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 175°C
- ④ Pulse width ≤ 1.0ms; duty cycle ≤ 2%.
- ⑤ C_{OSS eff.} is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DS}.
- ⑥ Limited by T_{Jmax}, see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑦ This value determined from sample failure population. 100% tested to this value in production.

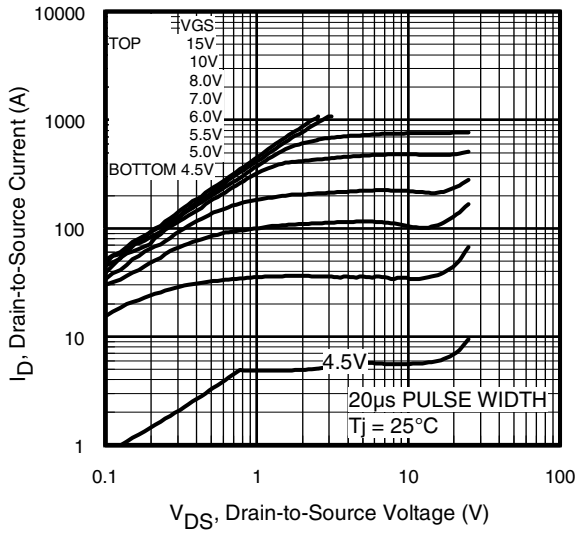


Fig 1. Typical Output Characteristics

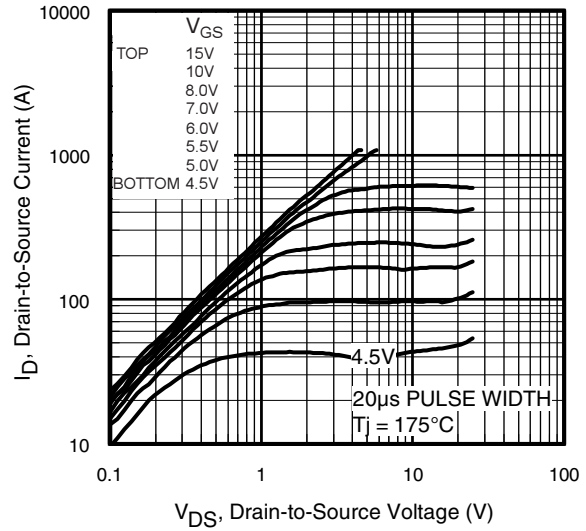


Fig 2. Typical Output Characteristics

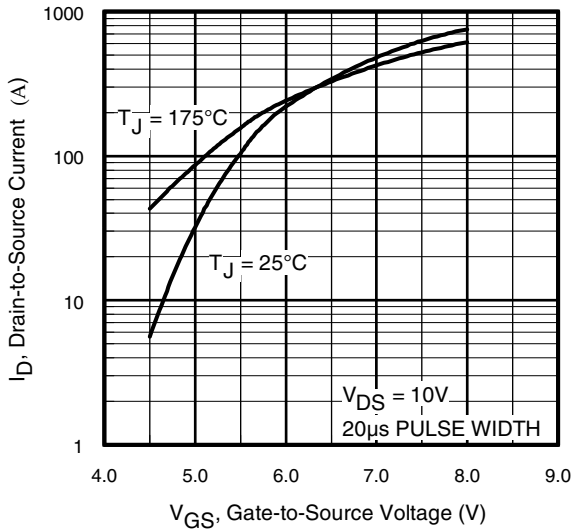


Fig 3. Typical Transfer Characteristics

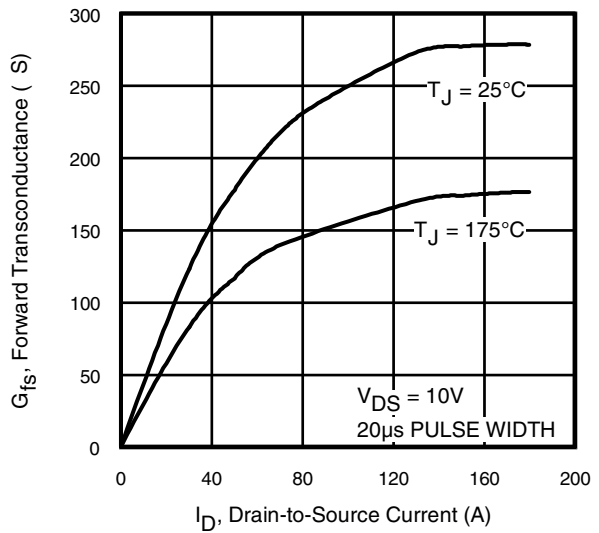


Fig 4. Typical Forward Transconductance Vs. Drain Current

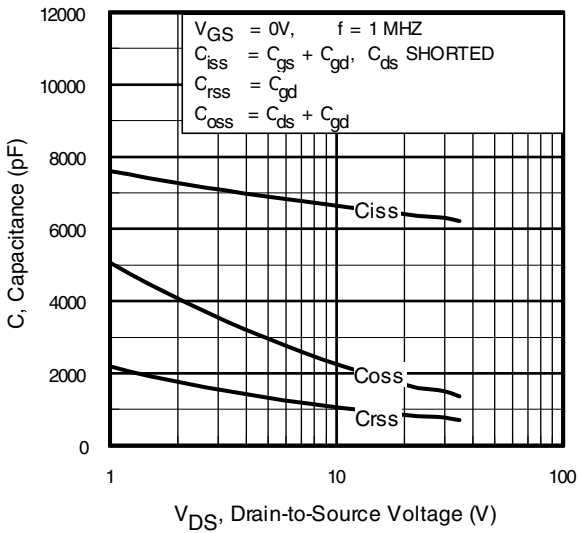


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

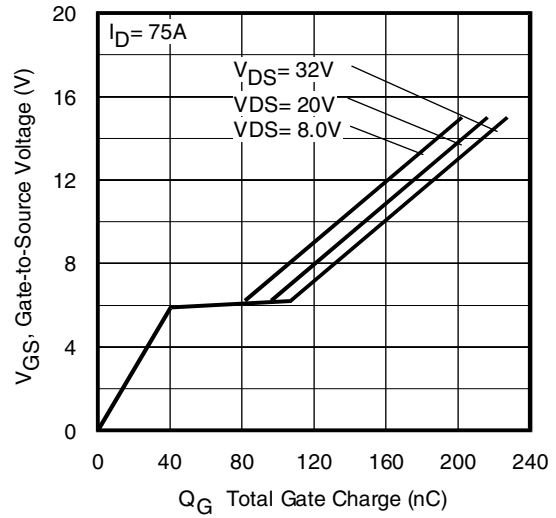


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

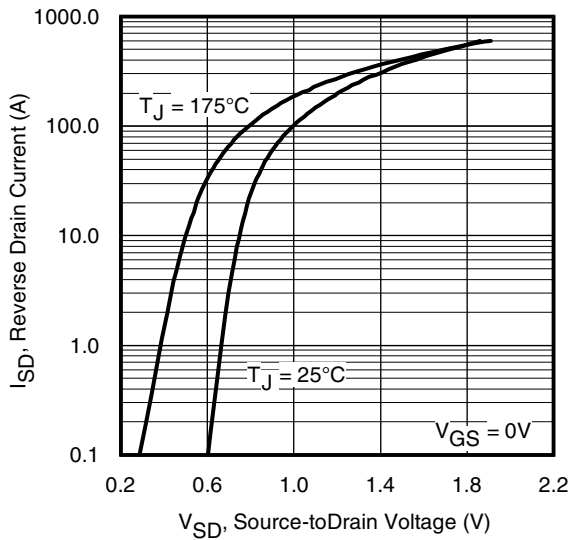


Fig 7. Typical Source-Drain Diode Forward Voltage

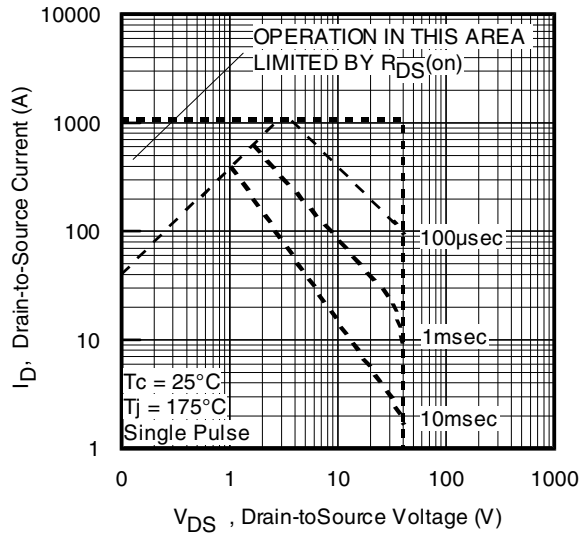


Fig 8. Maximum Safe Operating Area

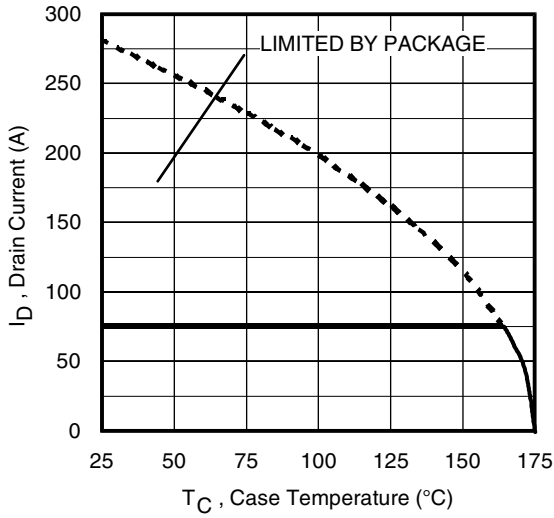


Fig 9. Maximum Drain Current Vs. Case Temperature

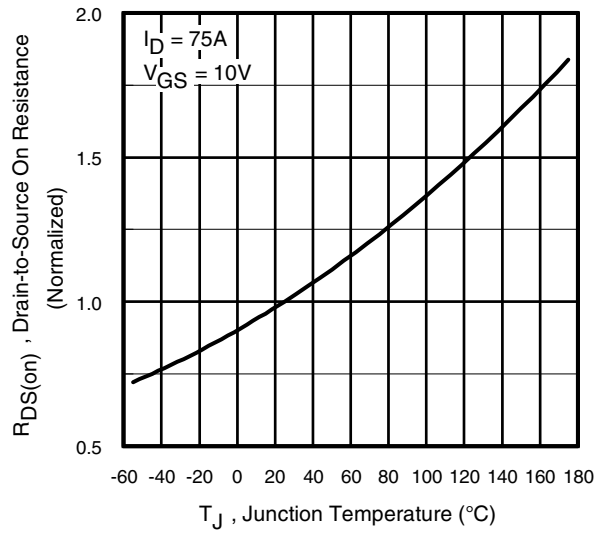


Fig 10. Normalized On-Resistance Vs. Temperature

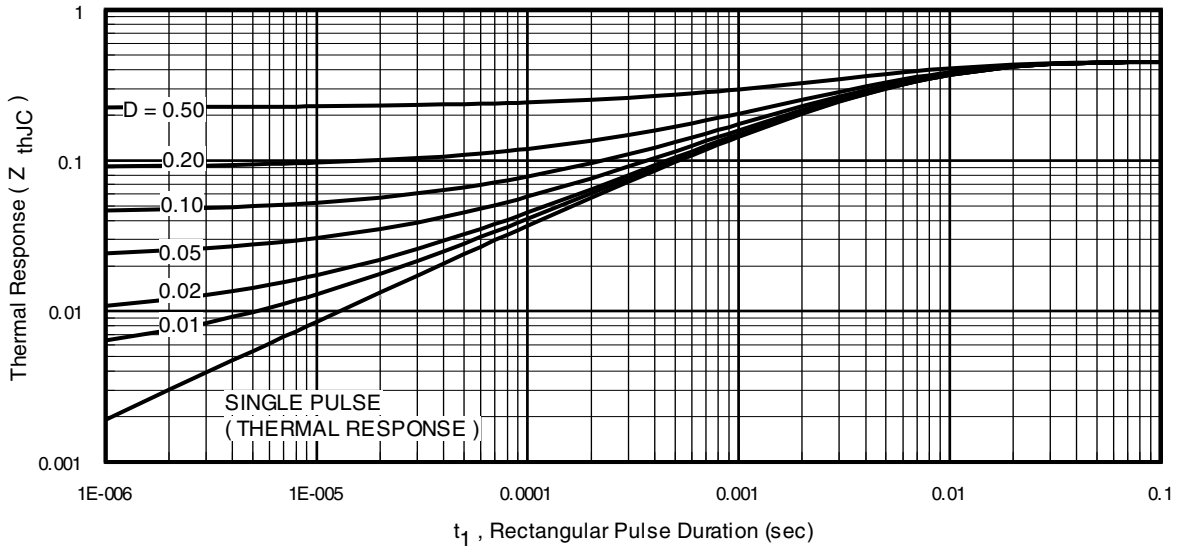


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

IRF2804

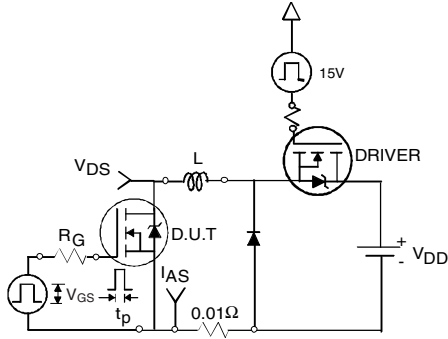


Fig 12a. Unclamped Inductive Test Circuit

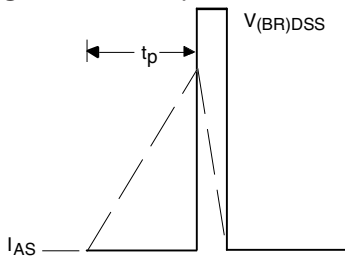


Fig 12b. Unclamped Inductive Waveforms

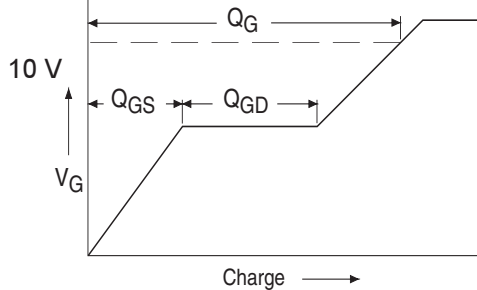


Fig 13a. Basic Gate Charge Waveform

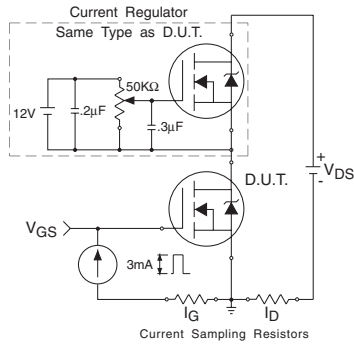


Fig 13b. Gate Charge Test Circuit

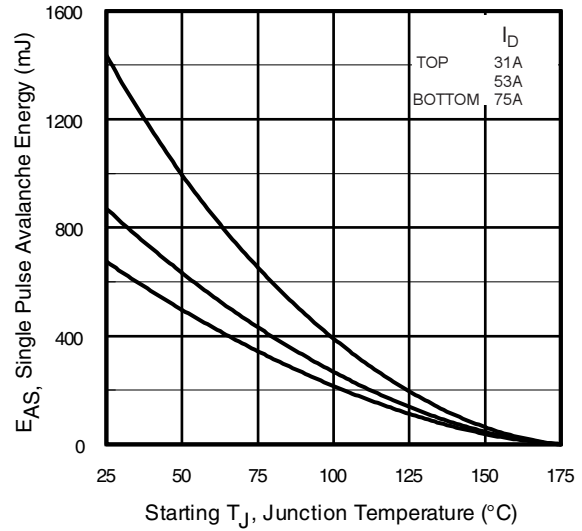


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

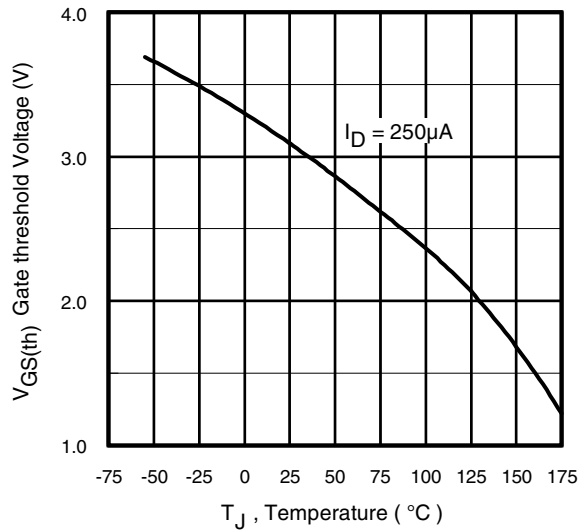


Fig 14. Threshold Voltage Vs. Temperature

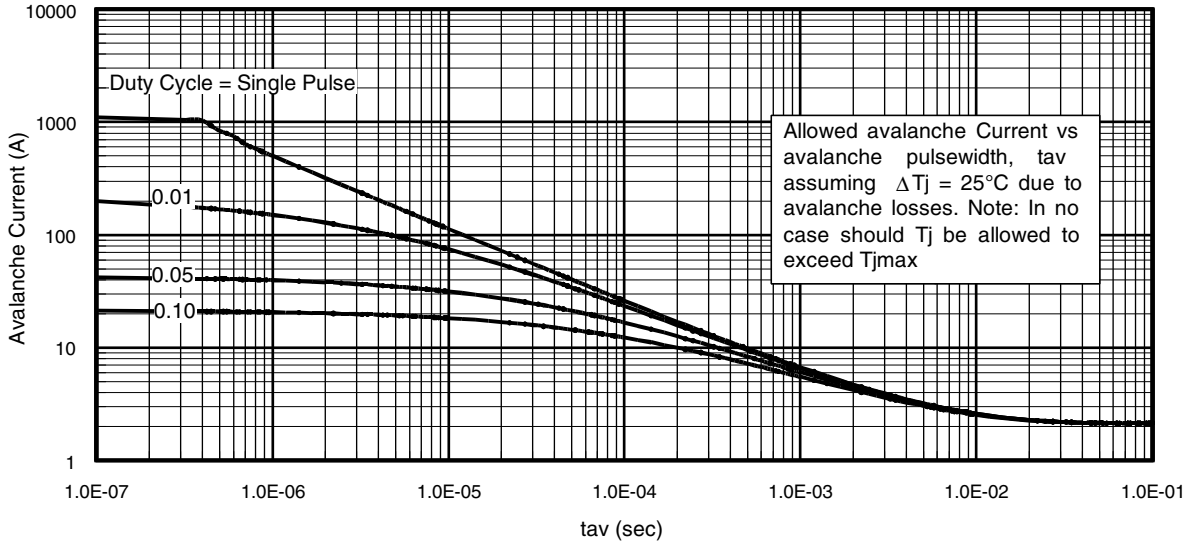


Fig 15. Typical Avalanche Current Vs.Pulsewidth

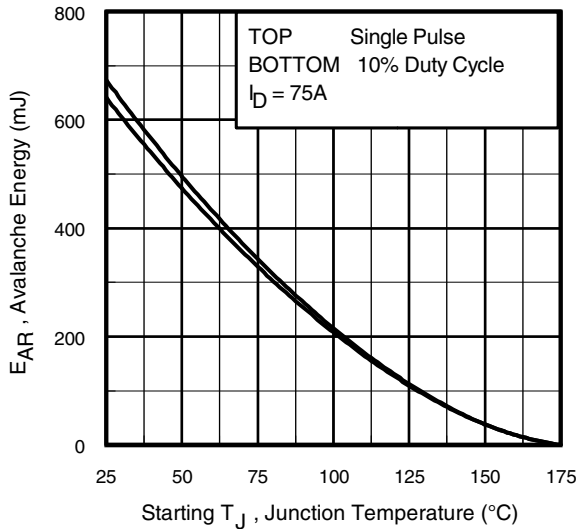


Fig 16. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

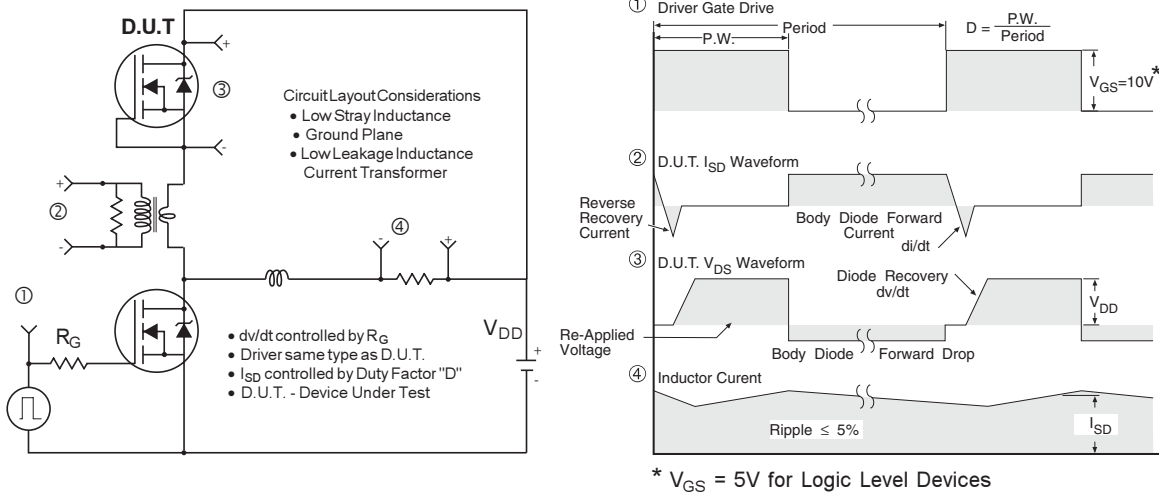


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

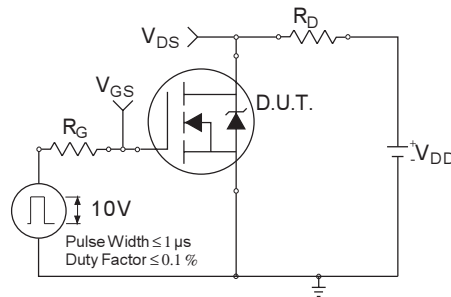


Fig 18a. Switching Time Test Circuit

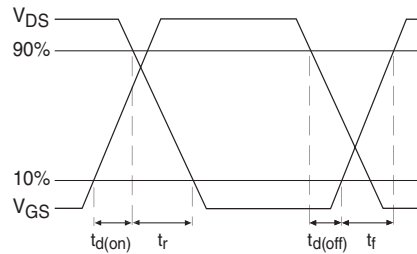
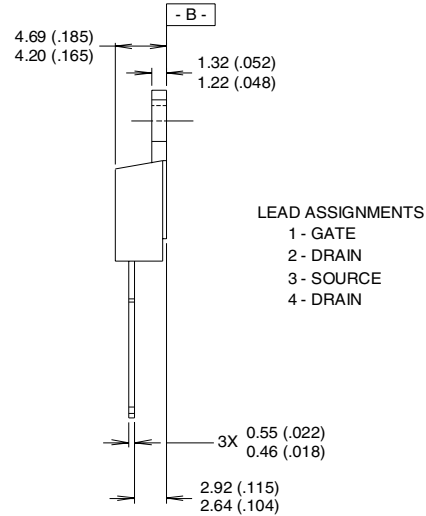
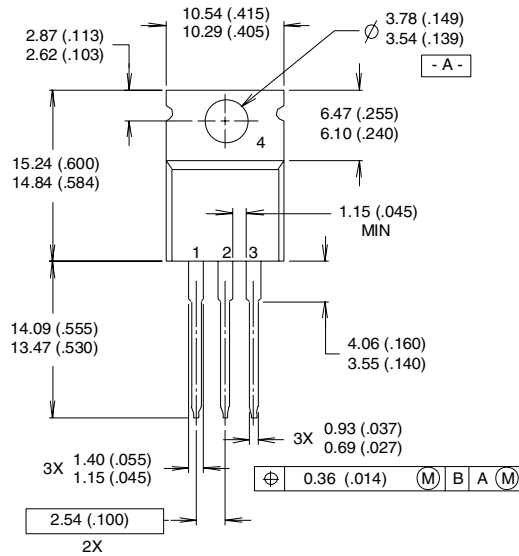


Fig 18b. Switching Time Waveforms

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)

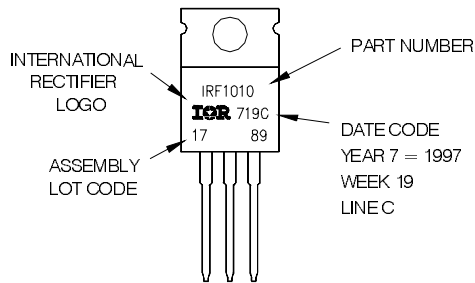


NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH
- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"



TO-220AB package is not recommended for Surface Mount Application.

Data and specifications subject to change without notice.
 This product has been designed and qualified for the Automotive [Q101] market.
 Qualification Standards can be found on IR's Web site.