



IRF740

N-CHANNEL 400V - 0.46Ω - 10A TO-220

PowerMESH™II MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
IRF740	400 V	< 0.55 Ω	10 A

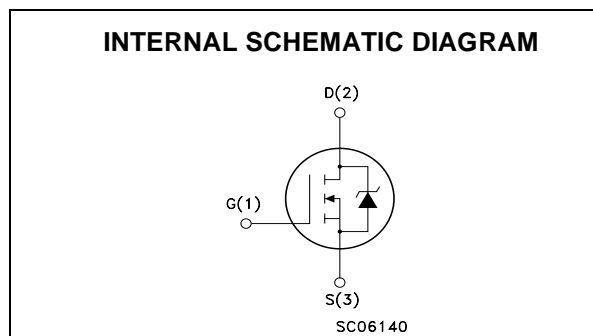
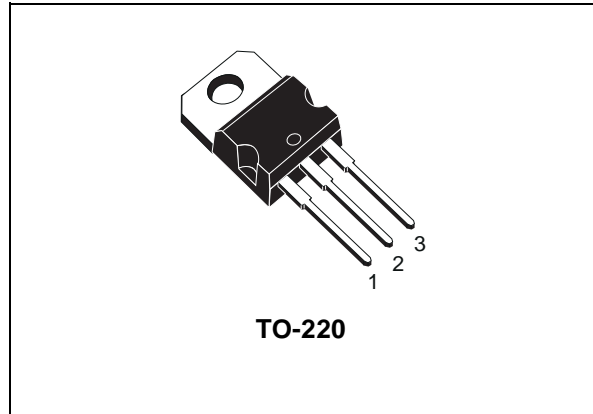
- TYPICAL R_{DS(on)} = 0.46Ω
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- LOW GATE CHARGE
- VERY LOW INTRINSIC CAPACITANCES

DESCRIPTION

The PowerMESH™II is the evolution of the first generation of MESH OVERLAY™. The layout refinements introduced greatly improve the Ron*area figure of merit while keeping the device at the leading edge for what concerns switching speed, gate charge and ruggedness.

APPLICATIONS

- HIGH-EFFICIENCY DC-DC CONVERTERS
- UPS AND MOTOR CONTROL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	400	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	400	V
V _{GS}	Gate- source Voltage	± 20	V
I _D	Drain Current (continuous) at T _C = 25°C	10	A
I _D	Drain Current (continuous) at T _C = 100°C	6.3	A
I _{DM} (●)	Drain Current (pulsed)	40	A
P _{TOT}	Total Dissipation at T _C = 25°C	125	W
	Derating Factor	1.0	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	4.0	V/ns
T _{stg}	Storage Temperature	- 65 to 150	°C
T _j	Max. Operating Junction Temperature		

(●) Pulse width limited by safe operating area

Note: NEW DATASHEET ACCORDING TO PCN DSG/CT/2C14.
SPECIAL MARKING: IRF740 @

(1) I_{SD} ≤ 10A, di/dt ≤ 120A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}.

IRF740

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	1	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
T _l	Maximum Lead Temperature For Soldering Purpose	300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	10	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	520	mJ

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED) OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	400			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 50	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ±20V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	2	3	4	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 5.3 A		0.46	0.55	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)} max, I _D = 6 A		7		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		1259		pF
C _{oss}	Output Capacitance			206		pF
C _{rss}	Reverse Transfer Capacitance			25.6		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 200V, I_D = 5 A$		17		ns
t_r	Rise Time	$R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 3)		10		ns
Q_g	Total Gate Charge	$V_{DD} = 320V, I_D = 10.7 A,$		35	43	nC
Q_{gs}	Gate-Source Charge	$V_{GS} = 10V$		11		nC
Q_{gd}	Gate-Drain Charge			12		nC

SWITCHING OFF

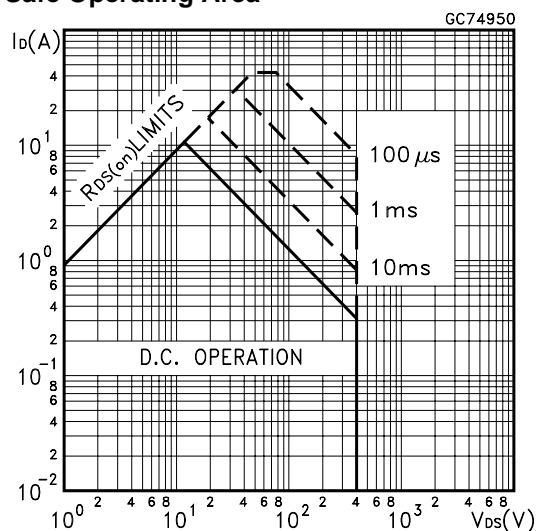
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Off-voltage Rise Time	$V_{clamp} = 320V, I_D = 10 A$		10		ns
t_f	Fall Time	$R_G = 4.7\Omega, V_{GS} = 10V$		10		ns
t_c	Cross-over Time	(see test circuit, Figure 5)		17		ns

SOURCE DRAIN DIODE

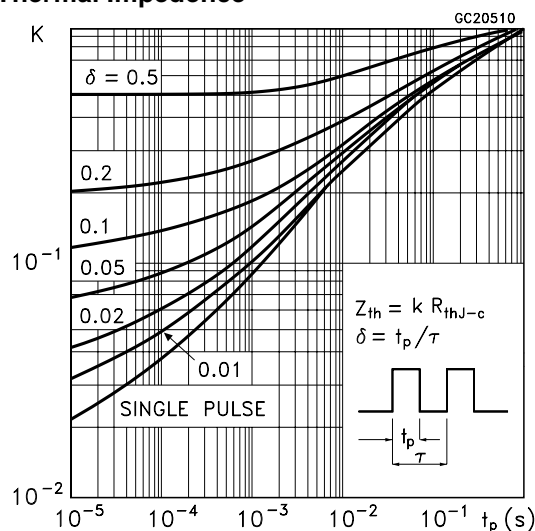
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				10	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				40	A
$V_{SD(1)}$	Forward On Voltage	$I_{SD} = 10 A, V_{GS} = 0$			1.6	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 10 A, di/dt = 100A/\mu s,$		370		ns
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 100V, T_j = 150^\circ C$		3.2		μC
I_{RRM}	Reverse Recovery Current	(see test circuit, Figure 5)		17		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
 2. Pulse width limited by safe operating area.

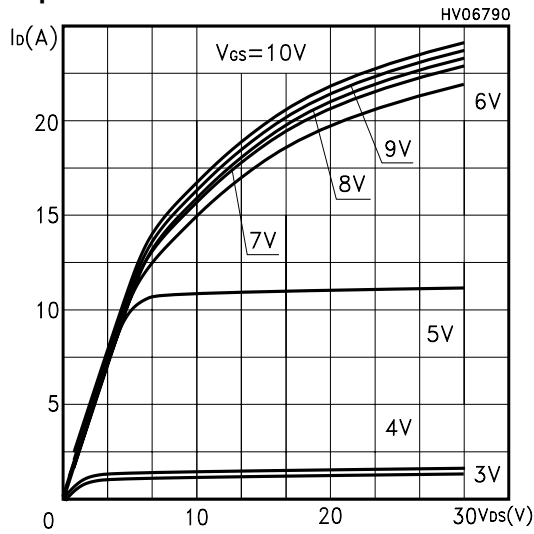
Safe Operating Area



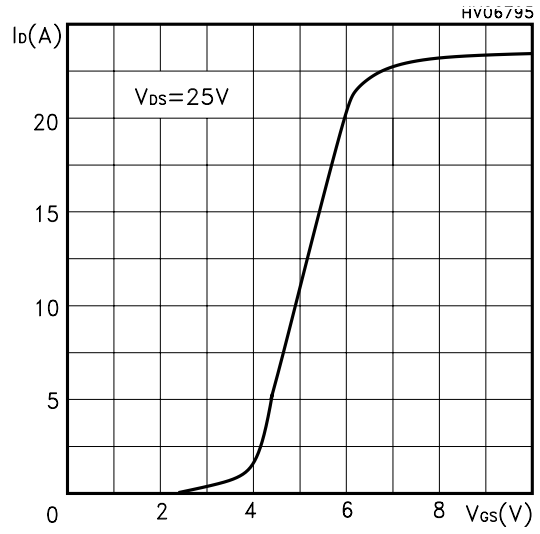
Thermal Impedance



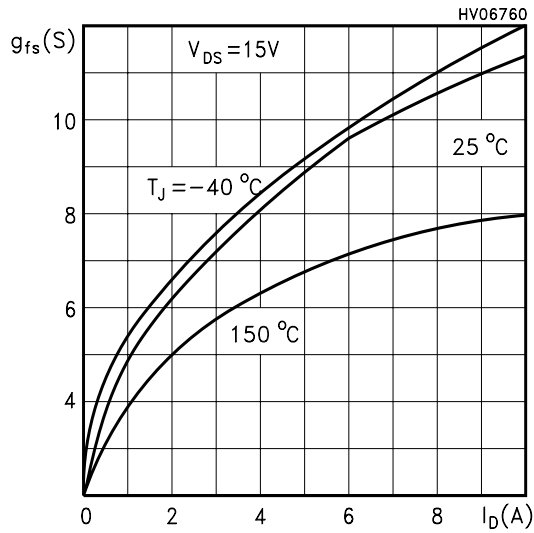
Output Characteristics



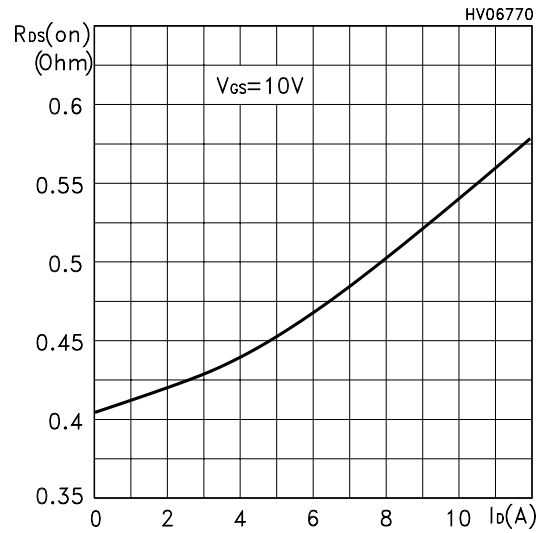
Transfer Characteristics



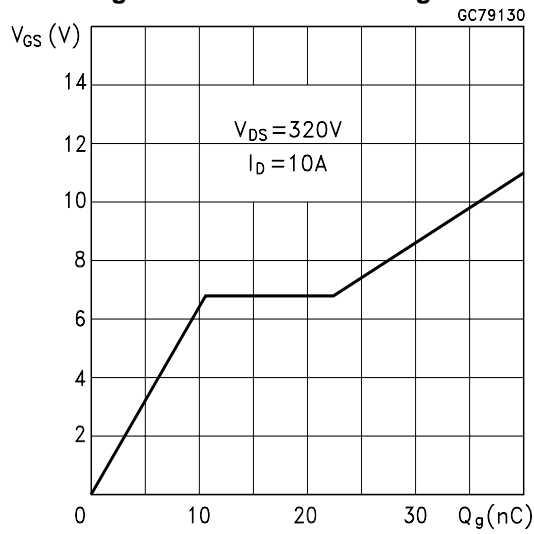
Transconductance



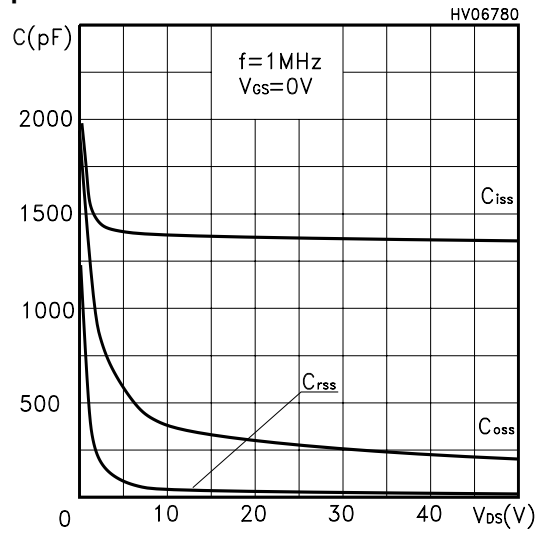
Static Drain-source On Resistance



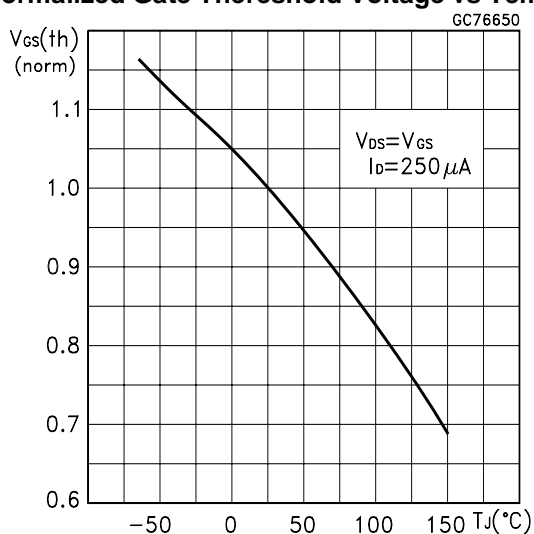
Gate Charge vs Gate-source Voltage



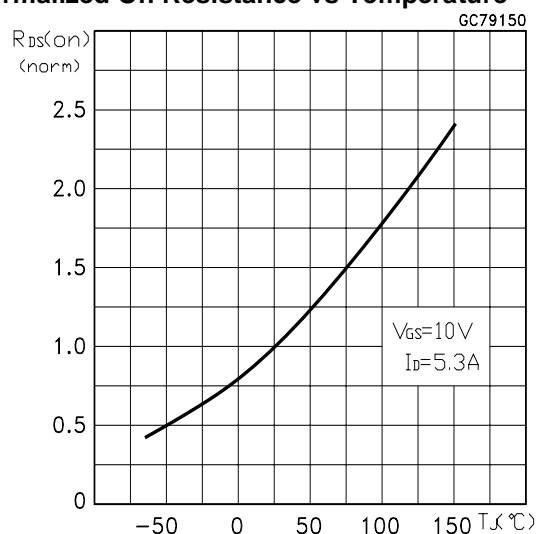
Capacitance Variations



Normalized Gate Threshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

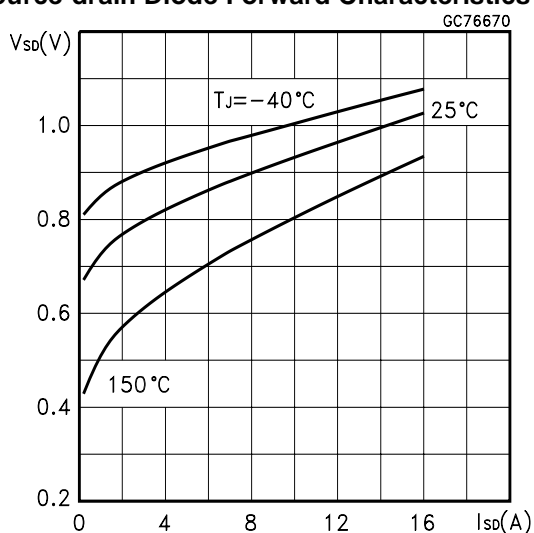


Fig. 1: Unclamped Inductive Load Test Circuit

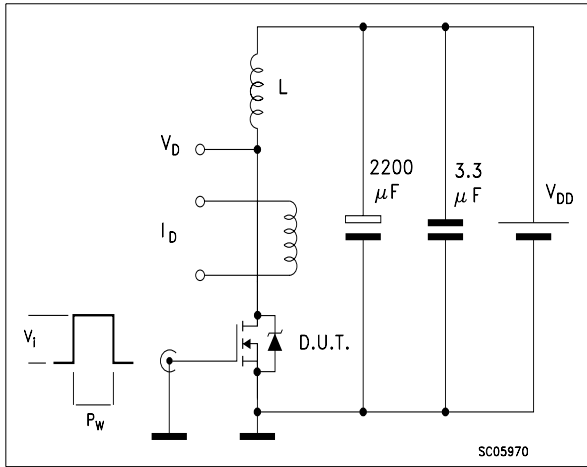


Fig. 2: Unclamped Inductive Waveform

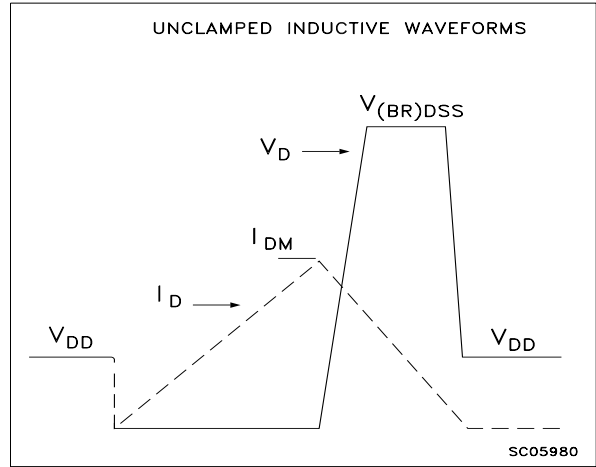


Fig. 3: Switching Times Test Circuit For Resistive Load

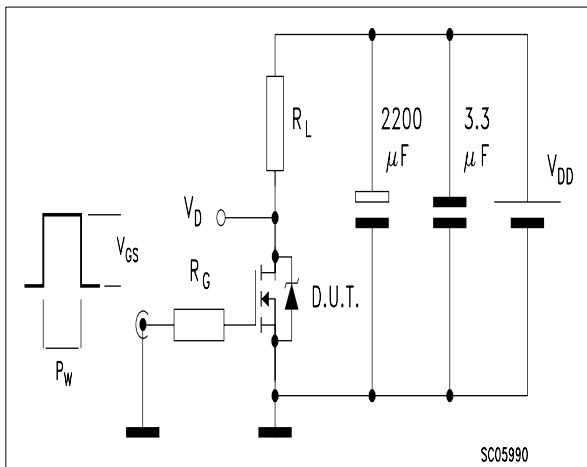


Fig. 4: Gate Charge test Circuit

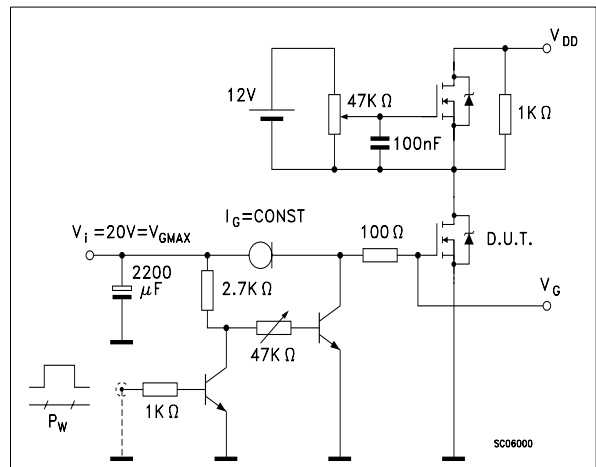
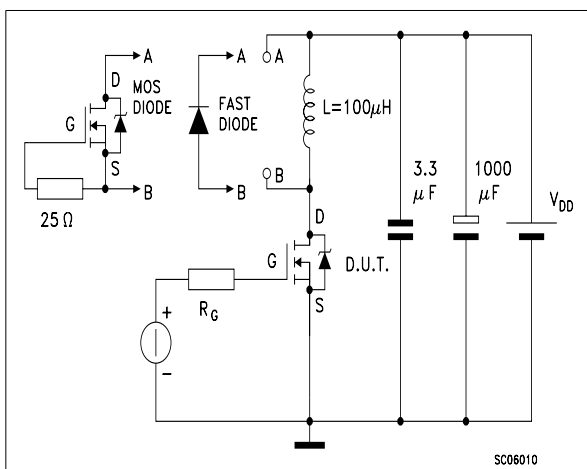
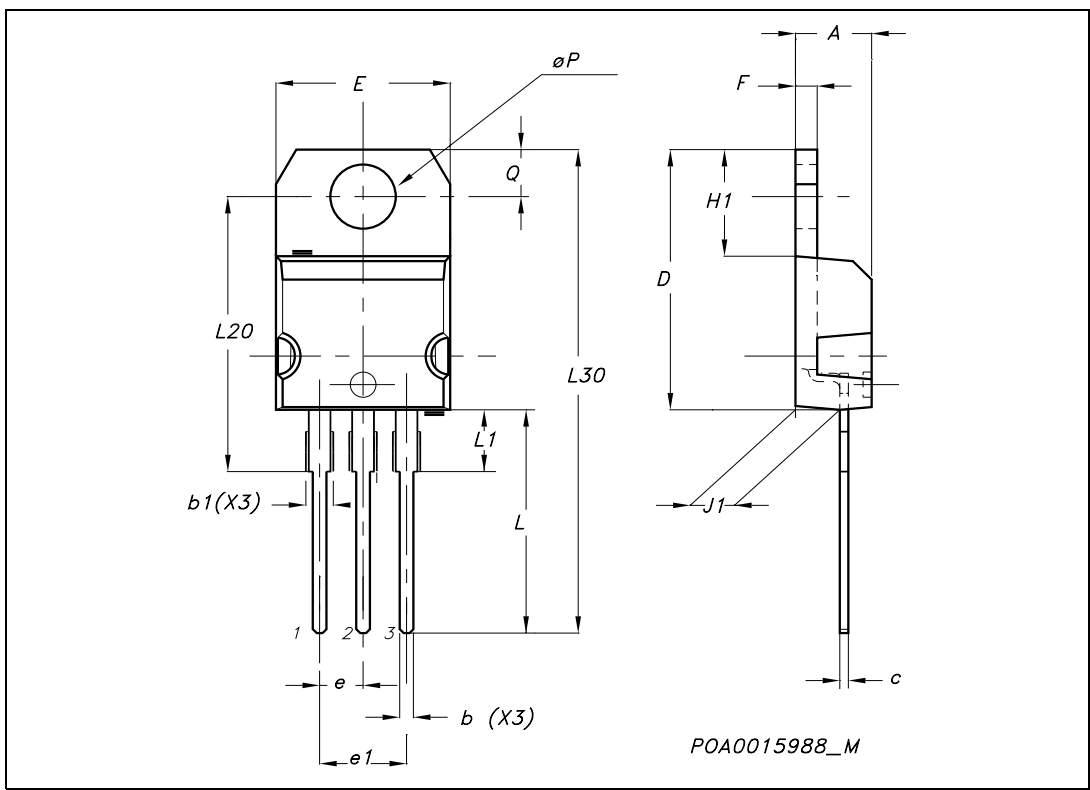


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



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