PD - 9.1319C

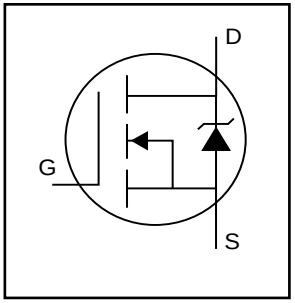
International
IOR Rectifier

PRELIMINARY

IRL3803S

HEXFET® Power MOSFET

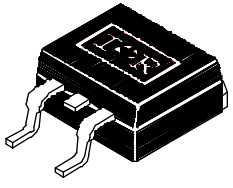
- Logic-Level Gate Drive
- Advanced Process Technology
- Surface Mount
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = 30V

$R_{DS(on)}$ = 0.006Ω

I_D = 120A⑤



D²Pak

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V⑥	120⑤	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V⑥	83⑤	
I_{DM}	Pulsed Drain Current ①⑥	470	
P_D @T_C = 25°C	Power Dissipation	150	W
	Linear Derating Factor	1.0	W/°C
V_{GS}	Gate-to-Source Voltage	±16	V
E_{AS}	Single Pulse Avalanche Energy ②⑥	610	mJ
I_{AR}	Avalanche Current①	71	A
E_{AR}	Repetitive Avalanche Energy①	15	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑥	1.8	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	——	1.0	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount,steady-state)**	——	——	40	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	30	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.052	—	V/°C	Reference to 25°C, I_D = 1mA⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.006	Ω	V_{GS} = 10V, I_D = 71A ④
		—	—	0.009		V_{GS} = 4.5V, I_D = 59A ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	—	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	55	—	—	S	V_{DS} = 25V, I_D = 71A⑥
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} = 30V, V_{GS} = 0V
		—	—	250		V_{DS} = 24V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 16V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -16V
Q_g	Total Gate Charge	—	—	140	nC	I_D = 71A
Q_{gs}	Gate-to-Source Charge	—	—	41		V_{DS} = 24V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	78		V_{GS} = 4.5V, See Fig. 6 and 13 ④⑥
$t_{d(on)}$	Turn-On Delay Time	—	14	—	ns	V_{DD} = 15V
t_r	Rise Time	—	230	—		I_D = 71A
$t_{d(off)}$	Turn-Off Delay Time	—	29	—		R_G = 1.3Ω, V_{GS} = 4.5V
t_f	Fall Time	—	35	—		R_D = 0.20Ω, See Fig. 10 ④⑥
L_S	Internal Source Inductance		7.5	—	nH	Between lead, and center of die contact
C_{iss}	Input Capacitance		5000		pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	1800	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	880	—		f = 1.0MHz, See Fig. 5⑥

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	120⑤	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	470		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 71A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	120	180	ns	T_J = 25°C, I_F = 71A
Q_{rr}	Reverse RecoveryCharge	—	450	680	nC	di/dt = 100A/µs ④⑥
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Specification changes

Rev. #	Parameters	Old spec.	New spec.	Comments	Revision Date
1	$V_{GS(th)}$ (Max.)	2.5V	No spec.	Removed $V_{GS(th)}$ Max. Specification	5/2/96
1	V_{GS} (Max.)	±20	±16	Decrease V_{GS} Max. Specification	5/2/96

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② V_{DD} = 15V, starting T_J = 25°C, L = 180µH R_G = 25Ω, I_{AS} = 71A. (See Figure 12)

③ I_{SD} ≤ 71A, di/dt ≤ 130A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ Caculated continuous current based on maximum allowable junction temperature;for recommended current-handling of the package refer to Design Tip # 93-4

⑥ Uses IRL3803 data and test conditions

** When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

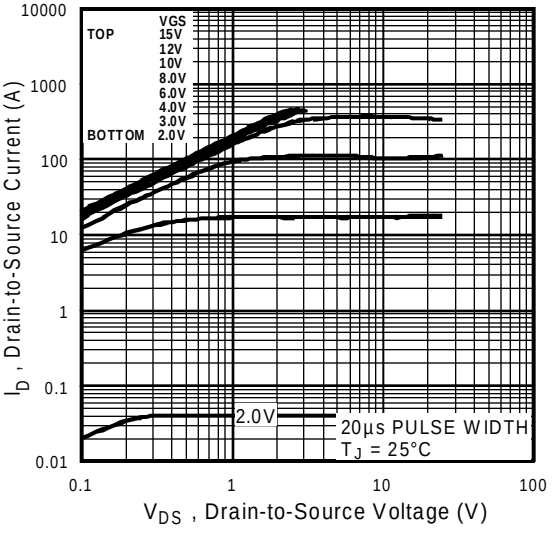


Fig 1. Typical Output Characteristics

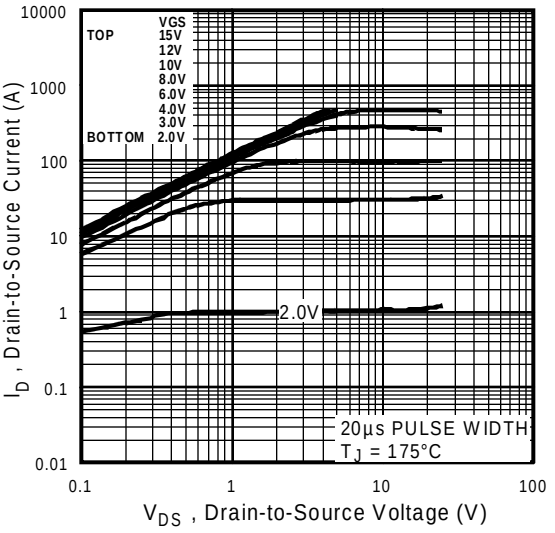


Fig 2. Typical Output Characteristics

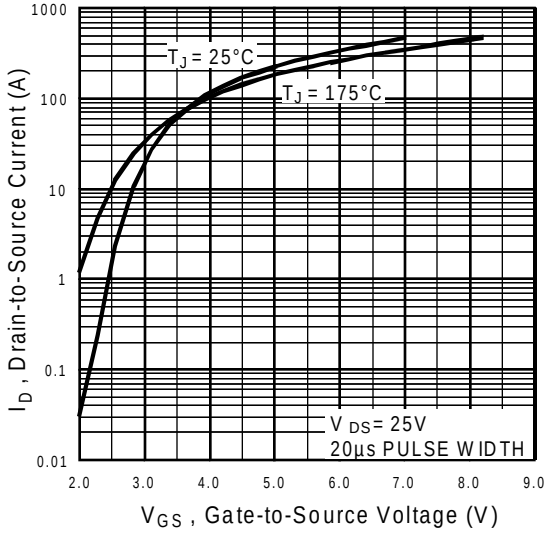


Fig 3. Typical Transfer Characteristics

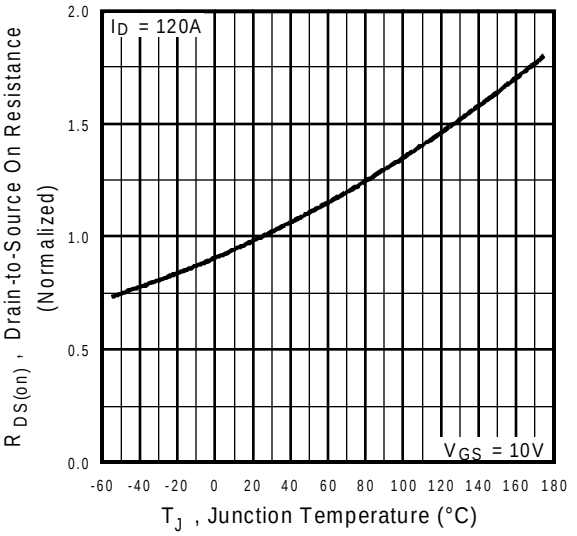


Fig 4. Normalized On-Resistance Vs. Temperature

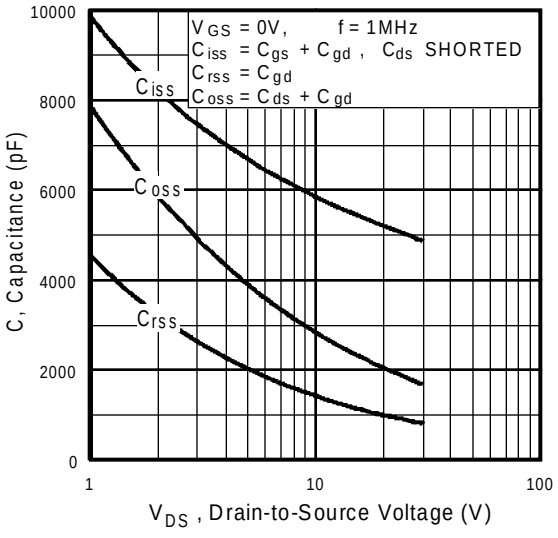


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

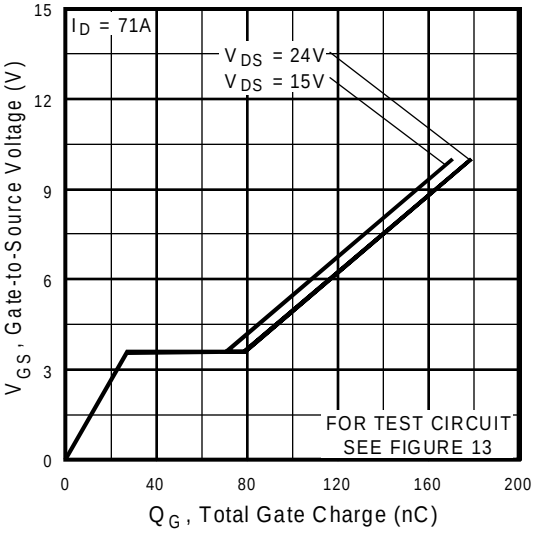


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

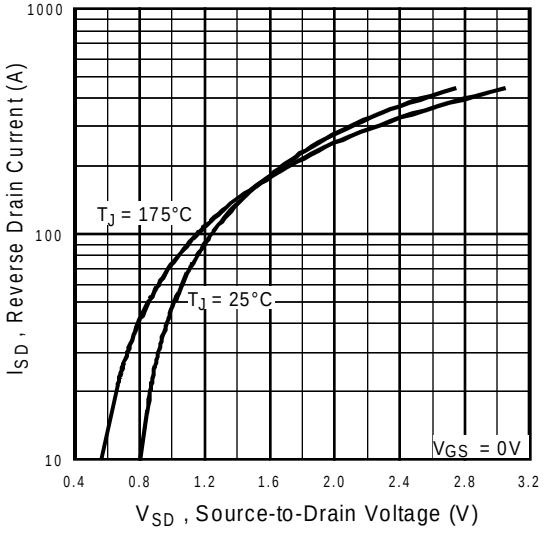


Fig 7. Typical Source-Drain Diode Forward Voltage

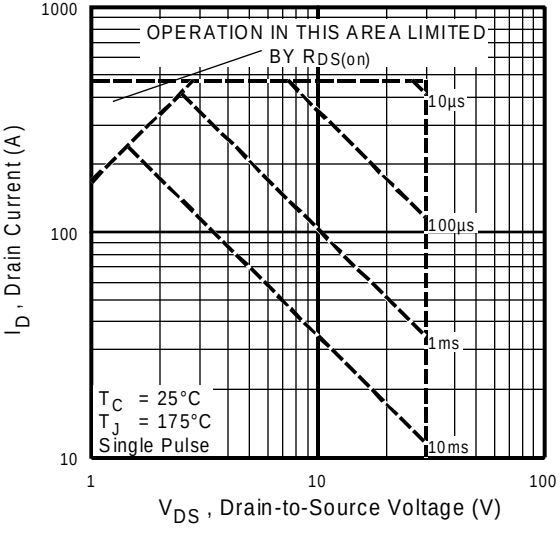


Fig 8. Maximum Safe Operating Area

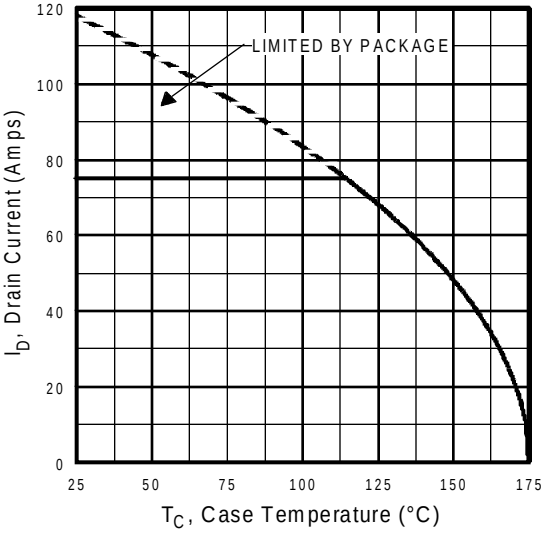


Fig 9. Maximum Drain Current Vs. Case Temperature

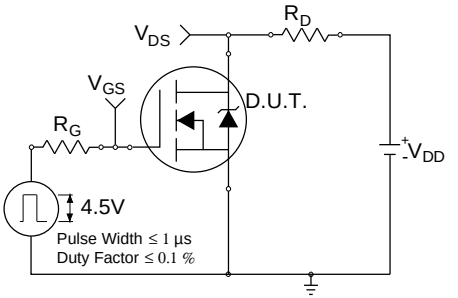


Fig 10a. Switching Time Test Circuit

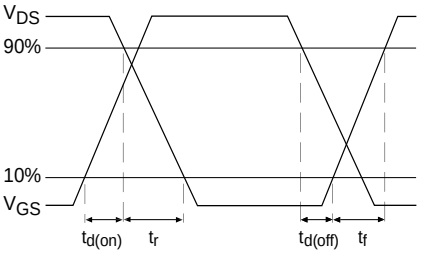


Fig 10b. Switching Time Waveforms

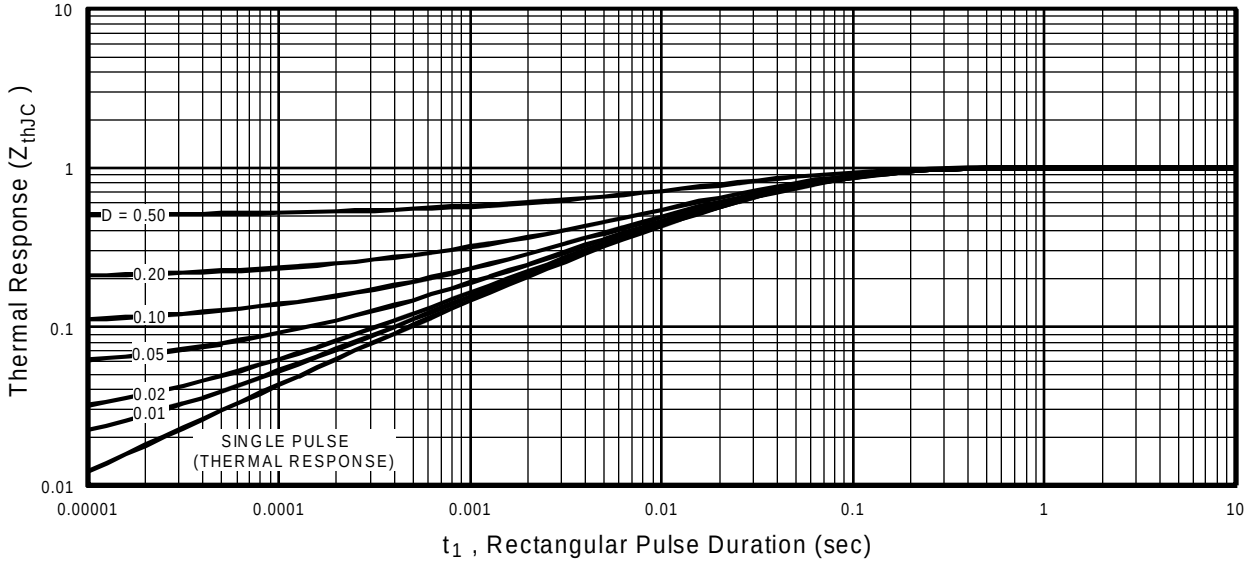


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

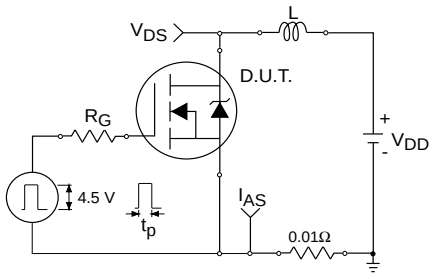


Fig 12a. Unclamped Inductive Test Circuit

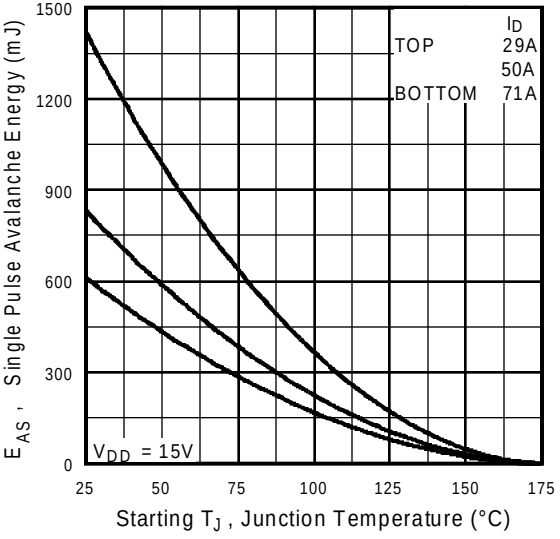


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

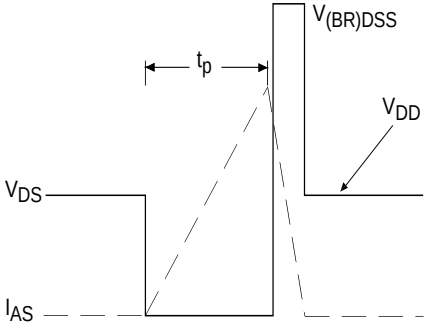


Fig 12b. Unclamped Inductive Waveforms

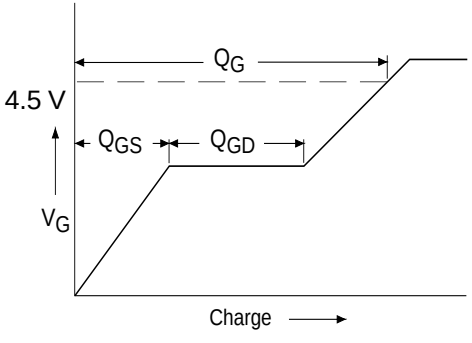


Fig 13a. Basic Gate Charge Waveform

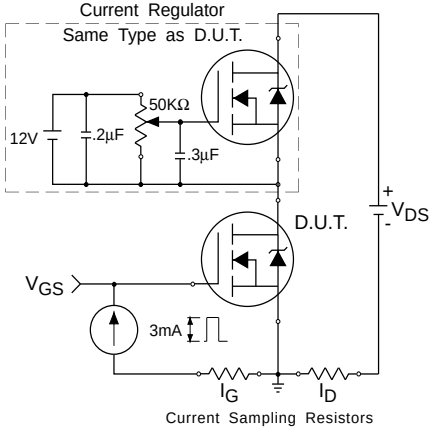
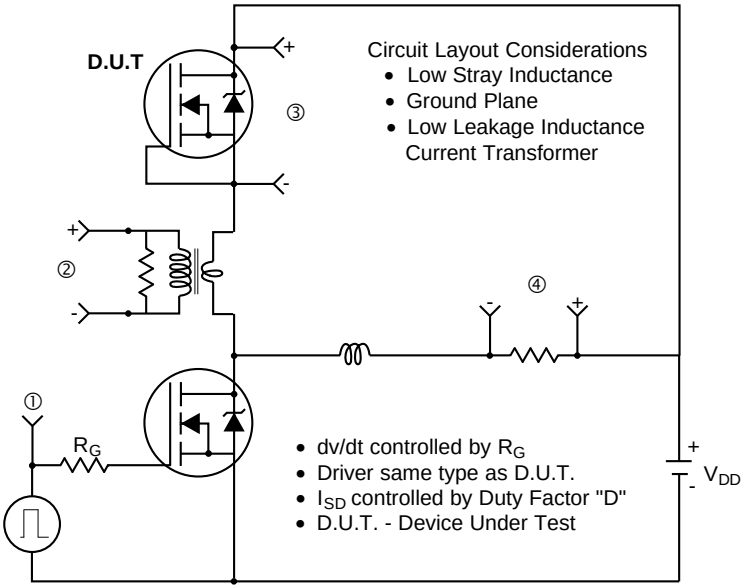
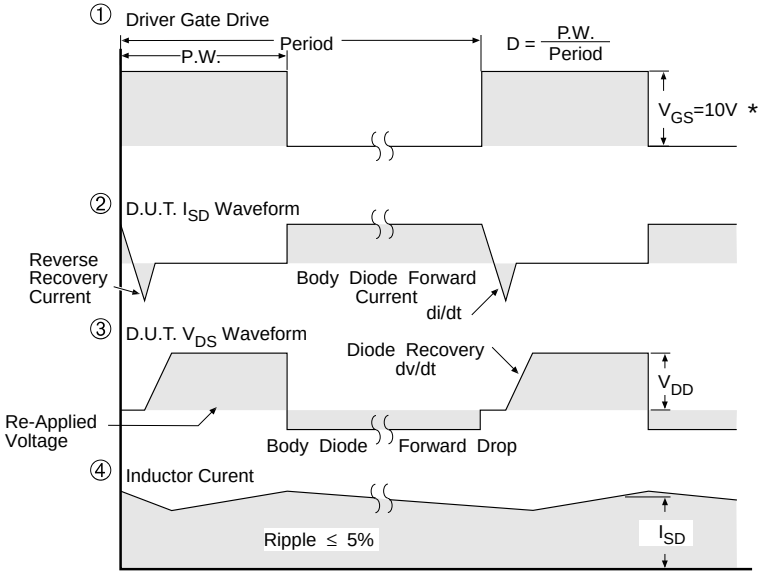


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit

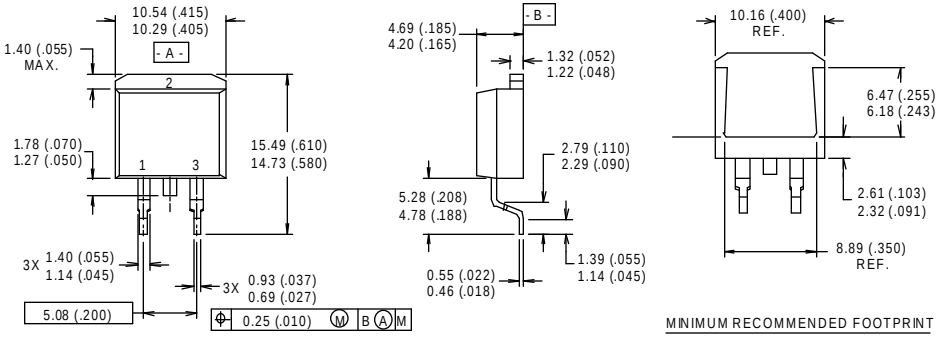




* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFETS

D²Pak Package Details



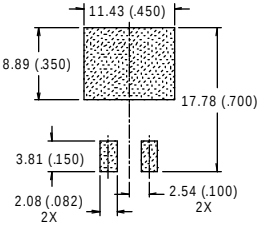
NOTES:

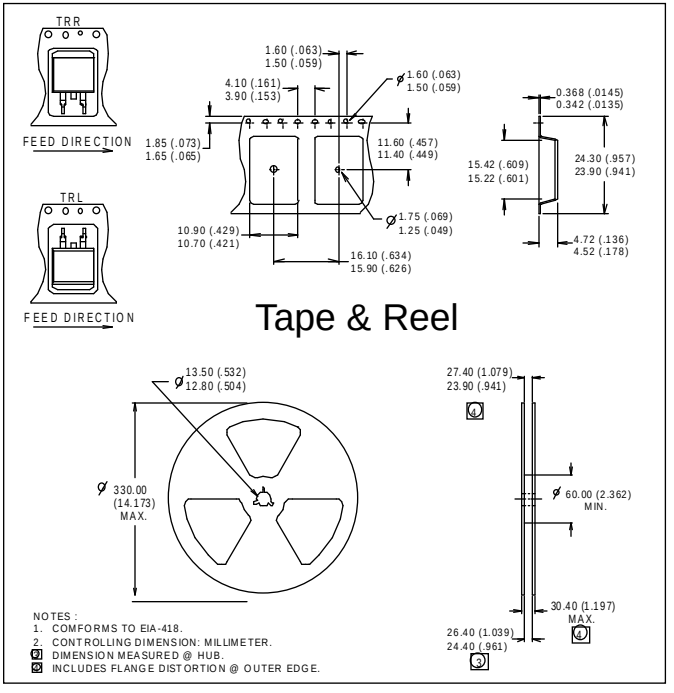
1 DIMENSIONS AFTER SOLDER DIP.
2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
3 CONTROLLING DIMENSION : INCH.
4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS

1 - GATE
2 - DRAIN
3 - SOURCE

MINIMUM RECOMMENDED FOOTPRINT

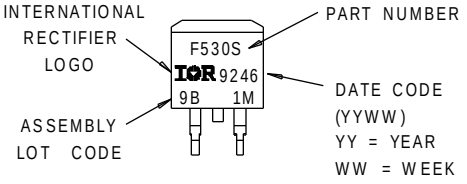




NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
DIMENSION MEASURED @ HUB.
INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Part Marking

(This is an IRF530S with assembly lot code 9B1M)



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