

# MN65761T

## Low Power 9-Bit CMOS A/D Converter for Image Processing

### ■ Overview

The MN65761T is a high-speed 9-bit CMOS analog-to-digital converter for image processing applications.

It uses a half flash structure based on chopper comparators and achieves both high speed and low power consumption with multiplexing.

It provides separate power supply pins for the circuits driving the low-voltage digital output pins.

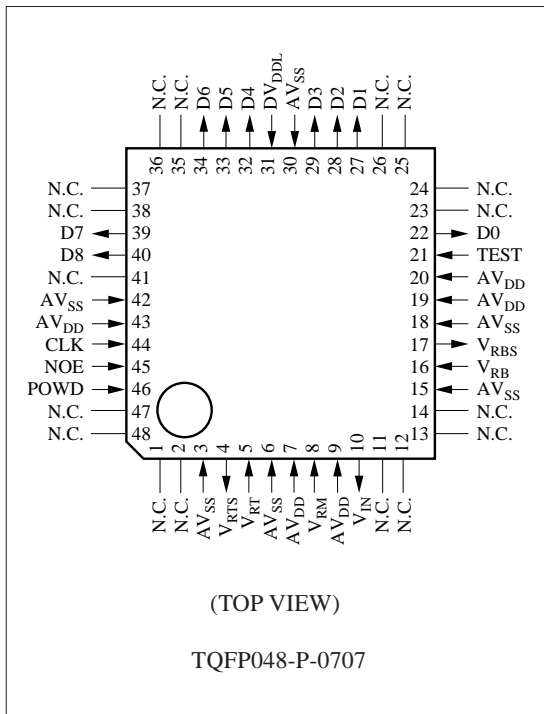
### ■ Features

- Maximum conversion rate: 18 MSPS (min.)
- Linearity error:  $\pm 1.3$  LSB (typ.)
- Differential linearity error:  $\pm 0.6$  LSB (typ.)
- Power supply voltage: 3.6 V or 2.6 V
- Power consumption: 60 mW (typ.) ( $f_{CLK}=18$  MHz)

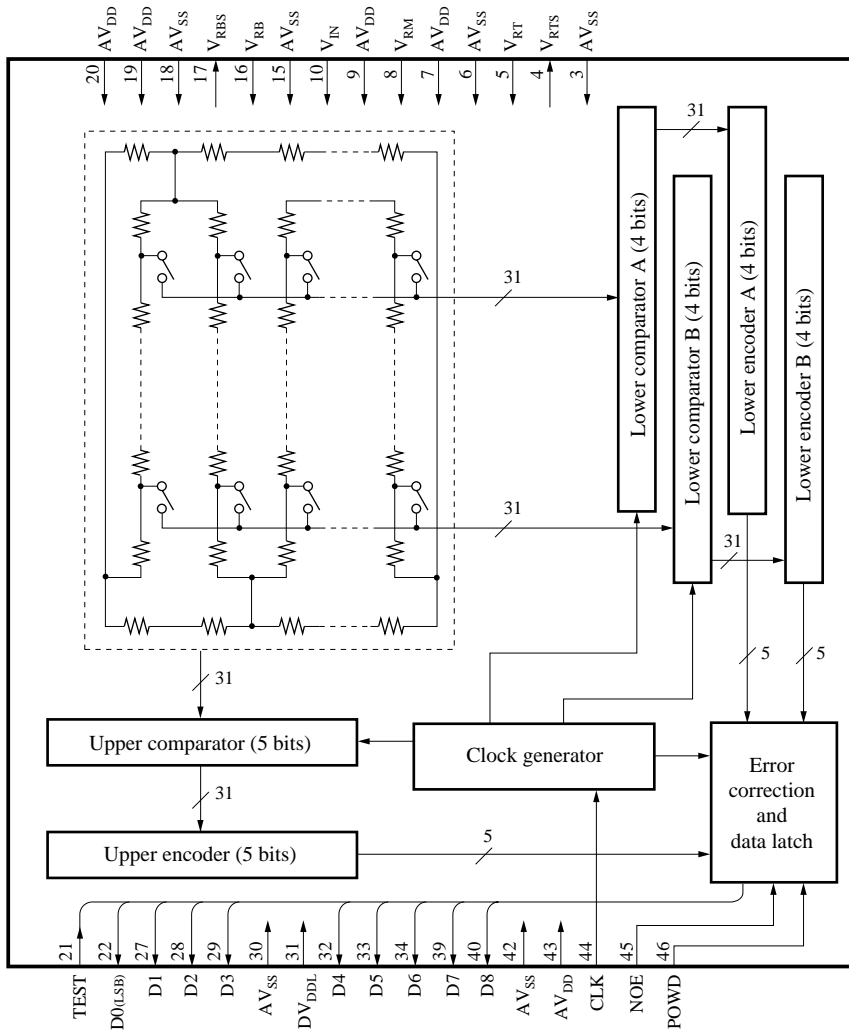
### ■ Applications

- Digital television receivers
- Digital video equipment
- Digital image processing equipment

### ■ Pin Assignment



■ Block Diagram



### ■ Pin Descriptions

Pin No.	Symbol	Function Description
1	N.C.	No connection
2	N.C.	No connection
3	AV <sub>SS</sub>	Ground for analog circuits
4	V <sub>RTS</sub>	Reference voltage power supply (TOP)
5	V <sub>RT</sub>	Reference voltage input (TOP)
6	AV <sub>SS</sub>	Ground for analog circuits
7	AV <sub>DD</sub>	Power supply for analog circuits
8	V <sub>RM</sub>	Intermediate reference voltage
9	AV <sub>DD</sub>	Power supply for analog circuits
10	V <sub>IN</sub>	Analog signal input
11	N.C.	No connection
12	N.C.	No connection
13	N.C.	No connection
14	N.C.	No connection
15	AV <sub>SS</sub>	Ground for analog circuits
16	V <sub>RB</sub>	Reference voltage input (BOTTOM)
17	V <sub>RBS</sub>	Reference voltage power supply (BOTTOM)
18	AV <sub>SS</sub>	Ground for analog circuits
19	AV <sub>DD</sub>	Power supply for analog circuits
20	AV <sub>DD</sub>	Power supply for analog circuits
21	TEST	Test mode selection
22	D0	Digital code output (LSB)
23	N.C.	No connection
24	N.C.	No connection
25	N.C.	No connection
26	N.C.	No connection
27	D1	Digital output
28	D2	Digital output
29	D3	Digital output
30	AV <sub>SS</sub>	Ground for analog circuits
31	DV <sub>DDL</sub>	Power supply for low-voltage digital outputs
32	D4	Digital output
33	D5	Digital output
34	D6	Digital output
35	N.C.	No connection
36	N.C.	No connection
37	N.C.	No connection
38	N.C.	No connection
39	D7	Digital output
40	D8	Digital output (MSB)

### ■ Pin Descriptions (continued)

Pin No.	Symbol	Function Description
41	N.C.	No connection
42	AV <sub>SS</sub>	Ground for analog circuits
43	AV <sub>DD</sub>	Power supply for analog circuits
44	CLK	Sampling clock
45	NOE	Digital output enable
46	POWD	Power down mode selection
47	N.C.	No connection
48	N.C.	No connection

### ■ Absolute Maximum Ratings Ta=25°C

Parameter	Symbol	Rating	Unit
Power supply voltage	V <sub>DD</sub>	- 0.3 to +7.0	V
Power supply voltage for digital output circuits	DV <sub>DDL</sub>	- 0.3 to V <sub>DD</sub> +0.3	V
Input voltage	V <sub>I</sub>	- 0.3 to V <sub>DD</sub> +0.3	V
Output voltage	V <sub>O</sub>	- 0.3 to V <sub>DD</sub> +0.3	V
Operating ambient temperature	T <sub>opr</sub>	-20 to +70	°C
Storage temperature	T <sub>stg</sub>	-55 to +125	°C

### ■ Recommended Operating Conditions V<sub>DD</sub>=AV<sub>DD</sub>=3.6V, DV<sub>DDL</sub>=2.6V, V<sub>SS</sub>=AV<sub>SS</sub>=0V, Ta=25°C

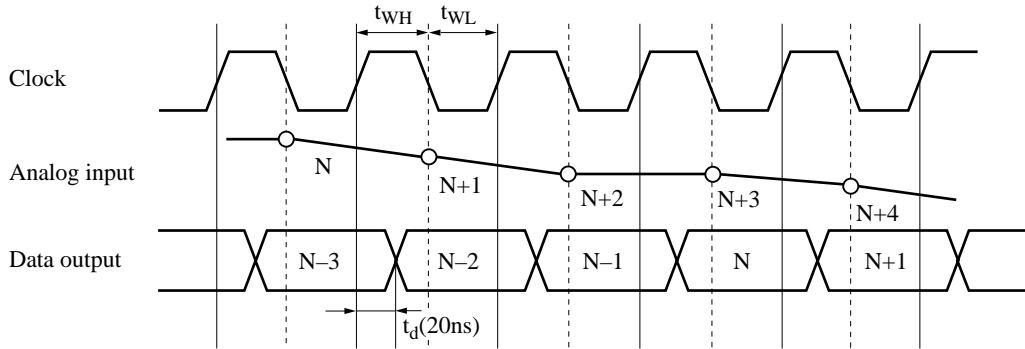
Parameter	Symbol	min	typ	max	Unit
Power supply voltage	V <sub>DD</sub>	3.15	3.60	3.70	V
Power supply voltage for digital output circuits	DV <sub>DDL</sub>	2.50	2.60	3.70	V
Digital input voltage	"H" level	V <sub>IH</sub>	AV <sub>DD</sub> × 0.55	AV <sub>DD</sub>	V
	"L" level	V <sub>IL</sub>	AV <sub>SS</sub>	AV <sub>DD</sub> × 0.20	V
Reference voltage	"H" level	V <sub>RT</sub>	3.30	AV <sub>DD</sub>	V
	"L" level	V <sub>RB</sub>	AV <sub>SS</sub>	1.30	V
Clock	"H" level pulse width	t <sub>WH</sub>	25		ns
	"L" level pulse width	t <sub>WL</sub>	25		ns
Analog input voltage	V <sub>AIN</sub>	AV <sub>SS</sub>		AV <sub>DD</sub>	V

### ■ Electrical Characteristics V<sub>DD</sub>=AV<sub>DD</sub>=3.6V, DV<sub>DDL</sub>=2.6V, AV<sub>SS</sub>=0V, Ta=25°C

Parameter	Symbol	Conditions	min	typ	max	Unit
Power consumption	P <sub>C</sub>	f <sub>CLK</sub> =18 MSPS (not including reference current)		60	100	mW
Resolution	RES	V <sub>DD</sub> =3.5V, DV <sub>DDL</sub> =2.5V		9		bit
Linearity error	E <sub>L</sub>	f <sub>CLK</sub> =18MSPS, V <sub>DD</sub> =3.5V		±1.3	±2.5	LSB
Differential linearity error	E <sub>D</sub>	V <sub>RT</sub> =3.3V, DV <sub>DDL</sub> =2.5V V <sub>RB</sub> =1.3V, CLK <sub>Duty</sub> =50±5%		±0.6	±1.0	LSB
Maximum conversion rate	F <sub>C(max.)</sub>	V <sub>DD</sub> =3.5V, DV <sub>DDL</sub> =2.5V	18			MSPS
Clock frequency	f <sub>CLK</sub>	V <sub>DD</sub> =3.5V, DV <sub>DDL</sub> =2.5V	1		18	MHz
Analog input dynamic range	D <sub>R</sub>	V <sub>DD</sub> =3.5V, DV <sub>DDL</sub> =2.5V	2		V <sub>RT</sub> -V <sub>RB</sub>	V
Output current	"H" level	I <sub>OH</sub>			-1.5	mA
	"L" level	I <sub>OL</sub>		1.5		mA
Output delay time	t <sub>d</sub>	Ta=70°C, C <sub>L</sub> =100Ω+10pF	10	20	35	ns
Analog input capacitance	C <sub>I</sub>	V <sub>IN</sub> pin		26		pF

**■ Timing Chart**

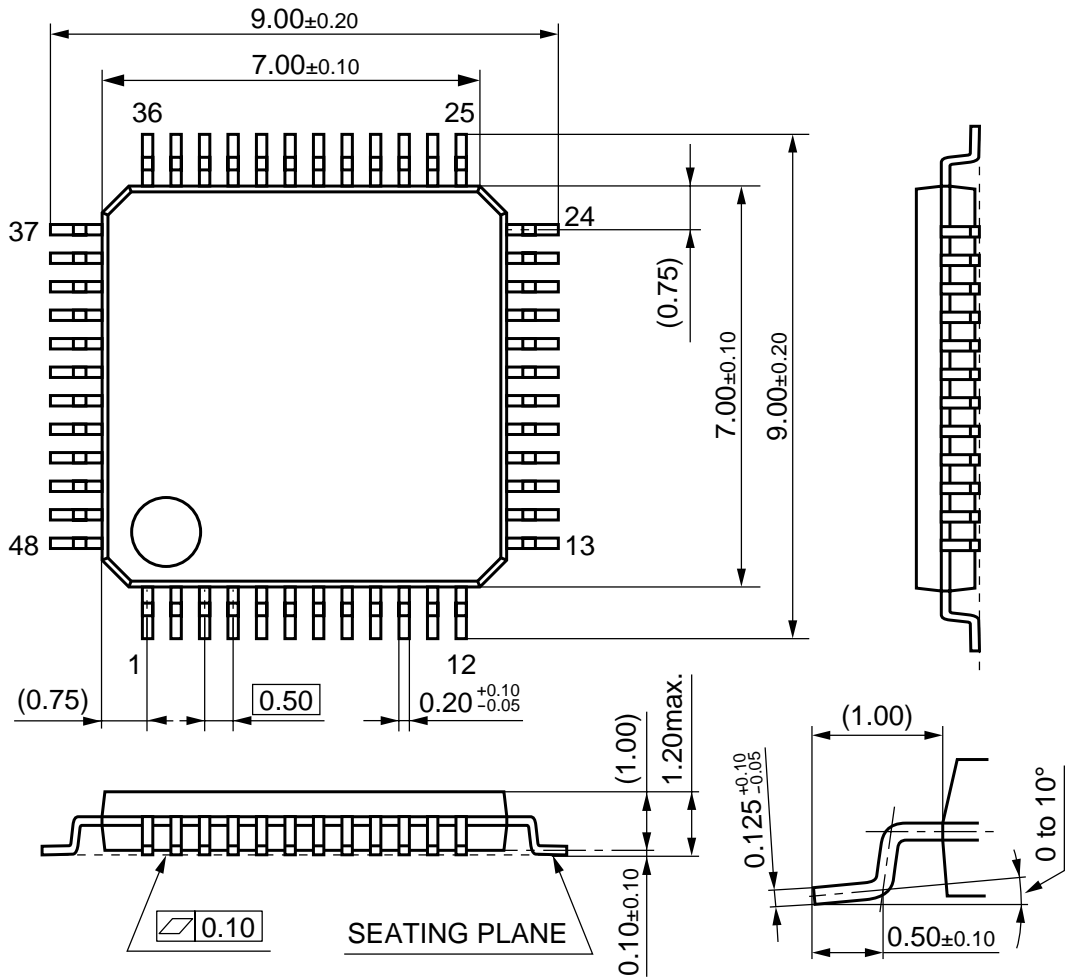
The chip samples the analog input at the falling edge of the clock signal and provides the corresponding digital output 2.5 clock cycles later at the rising edge of the clock signal.



Note: The circles indicate analog signal sampling points.

■ Package Dimensions (Unit:mm)

TQFP048-P-0707



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