



## Low-Noise, High-Precision, JFET-Input OPERATIONAL AMPLIFIER

Check for Samples: [OPA827](#)

### FEATURES

- **INPUT VOLTAGE NOISE DENSITY:**  
4nV/√Hz at 1kHz
- **INPUT VOLTAGE NOISE:**  
0.1Hz to 10Hz: 250nV<sub>PP</sub>
- **INPUT BIAS CURRENT:** 10pA (max)
- **INPUT OFFSET VOLTAGE:** 150μV (max)
- **INPUT OFFSET DRIFT:** 2.0μV/°C (max)
- **GAIN BANDWIDTH:** 22MHz
- **SLEW RATE:** 28V/μs
- **QUIESCENT CURRENT:** 4.8mA/Ch
- **WIDE SUPPLY RANGE:** ±4V to ±18V
- **PACKAGES:** SO-8 and MSOP-8

### APPLICATIONS

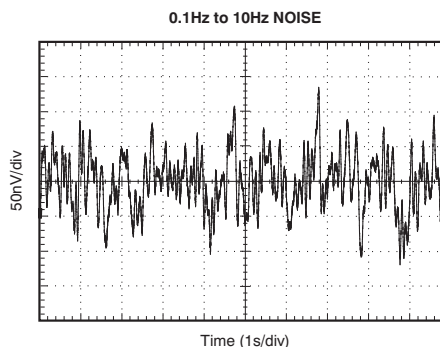
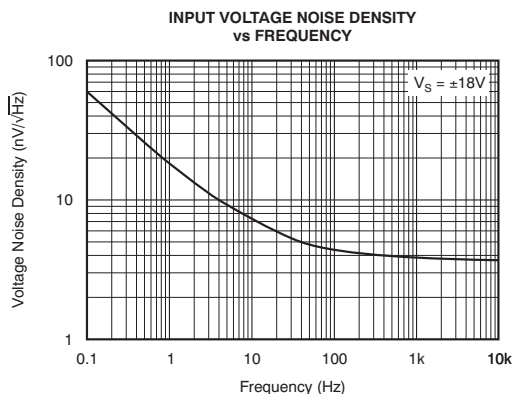
- ADC DRIVERS
- DAC OUTPUT BUFFERS
- TEST EQUIPMENT
- MEDICAL EQUIPMENT
- PLL FILTERS
- SEISMIC APPLICATIONS
- TRANSIMPEDANCE AMPLIFIERS
- INTEGRATORS
- ACTIVE FILTERS

### DESCRIPTION

The OPA827 series of JFET operational amplifiers combine outstanding dc precision with excellent ac performance. These amplifiers offer low offset voltage (150μV, max), very low drift over temperature (0.5μV/°C, typ), low bias current (3pA, typ), and very low 0.1Hz to 10Hz noise (250nV<sub>PP</sub>, typ). The device operates over a wide supply voltage range, ±4V to ±18V on a low supply current (4.8mA/Ch, typ).

Excellent ac characteristics, such as a 22MHz gain bandwidth product (GBW), a slew rate of 28V/μs, and precision dc characteristics make the OPA827 series well-suited for a wide range of applications including 16-bit to 18-bit mixed signal systems, transimpedance (I/V-conversion) amplifiers, filters, precision ±10V front ends, and professional audio applications.

The OPA827 is available in both SO-8 and MSOP-8 surface-mount packages, and is specified from –40°C to +125°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### PACKAGE/ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
<b>Standard Grade</b>			
OPA827AI	SO-8	D	OPA827A
OPA827AI	MSOP-8	DGK	NSP

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		VALUE	UNIT
Supply Voltage	$V_S = (V_+) - (V_-)$	40	V
Input Voltage <sup>(2)</sup>		$(V_-) - 0.5$ to $(V_+) + 0.5$	V
Input Current <sup>(2)</sup>		$\pm 10$	mA
Differential Input Voltage		$\pm V_S$	V
Output Short-Circuit <sup>(3)</sup>		Continuous	
Operating Temperature	$T_A$	-55 to +150	°C
Storage Temperature	$T_A$	-65 to +150	°C
Junction Temperature	$T_J$	+150	°C
ESD Ratings	Human Body Model (HBM)	4000	V
	Charged Device Model (CDM)	1000	V

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less.
- (3) Short-circuit to  $V_S/2$  (ground in symmetrical dual-supply setups).

**ELECTRICAL CHARACTERISTICS:  $V_S = \pm 4V$  to  $\pm 18V$** 
**Boldface** limits apply over the specified temperature range,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ .

At  $T_A = +25^\circ\text{C}$ ,  $R_L = 10\text{k}\Omega$  connected to midsupply,  $V_{CM} = V_{OUT} = \text{midsupply}$ , unless otherwise noted.

PARAMETER	CONDITIONS	OPA827AI			UNIT
		MIN	TYP	MAX	
<b>OFFSET VOLTAGE</b>					
Input Offset Voltage	$V_{OS}$ $V_S = \pm 15V, V_{CM} = 0V$		75	150	$\mu\text{V}$
Drift	$dV_{OS}/dT$		<b>0.1</b>	<b>2.0</b>	$\mu\text{V}/^\circ\text{C}$
vs Power Supply	PSRR		0.2	1	$\mu\text{V}/\text{V}$
<b>Over Temperature</b>				<b>3</b>	$\mu\text{V}/\text{V}$
<b>INPUT BIAS CURRENT</b>					
Input Bias Current	$I_B$  $-40^\circ\text{C}$ to $+85^\circ\text{C}$ <b><math>-40^\circ\text{C}</math> to <math>+125^\circ\text{C}</math></b>		$\pm 3$	$\pm 10$ $\pm 500$	pA pA <b>nA</b>
<b>Over Temperature</b>				<b><math>\pm 5</math></b>	<b>nA</b>
Input Offset Current	$I_{OS}$		$\pm 3$	$\pm 10$	pA
<b>NOISE</b>					
Input Voltage Noise:					
f = 0.1Hz to 10Hz	$e_n$ $V_S = \pm 18V, V_{CM} = 0V$		250		nV <sub>PP</sub>
Input Voltage Noise Density:					
f = 1kHz	$e_n$ $V_S = \pm 18V, V_{CM} = 0V$		4		nV/ $\sqrt{\text{Hz}}$
f = 10kHz	$e_n$ $V_S = \pm 18V, V_{CM} = 0V$		3.8		nV/ $\sqrt{\text{Hz}}$
Input Current Noise Density:					
f = 1kHz	$i_n$ $V_S = \pm 18V, V_{CM} = 0V$		2.2		fA/ $\sqrt{\text{Hz}}$
<b>INPUT VOLTAGE RANGE</b>					
Common-Mode Voltage Range	$V_{CM}$	(V-)+3		(V+)-3	V
Common-Mode Rejection Ratio	CMRR $(V-)+3V \leq V_{CM} \leq (V+)-3V, V_S < 10V$	104	114		dB
	$(V-)+3V \leq V_{CM} \leq (V+)-3V, V_S \geq 10V$	114	126		dB
<b>Over Temperature</b>	<b><math>(V-)+3V \leq V_{CM} \leq (V+)-3V, V_S &lt; 10V</math></b>	<b>100</b>			<b>dB</b>
	<b><math>(V-)+3V \leq V_{CM} \leq (V+)-3V, V_S \geq 10V</math></b>	<b>110</b>			<b>dB</b>
<b>INPUT IMPEDANCE</b>					
Differential			$10^{13} \parallel 9$		$\Omega \parallel \text{pF}$
Common-Mode			$10^{13} \parallel 9$		$\Omega \parallel \text{pF}$
<b>OPEN-LOOP GAIN</b>					
Open-Loop Voltage Gain	$A_{OL}$ $(V-)+3V \leq V_O \leq (V+)-3V, R_L = 1\text{k}\Omega$	120	126		dB
<b>Over Temperature</b>	<b><math>(V-)+3V \leq V_O \leq (V+)-3V, R_L = 1\text{k}\Omega</math></b>	<b>114</b>			<b>dB</b>
<b>FREQUENCY RESPONSE</b>					
Gain-Bandwidth Product	GBW G = +1		22		MHz
Slew Rate	SR G = -1	20	28		V/ $\mu\text{s}$
Settling Time, $\pm 0.01\%$	$t_s$ 10V Step, G = -1, $C_L = 100\text{pF}$		550		ns
0.00075% (16-bit)	10V Step, G = -1, $C_L = 100\text{pF}$		850		ns
Overload Recovery Time	Gain = -10		150		ns
Total Harmonic Distortion + Noise	THD+N G = +1, f = 1kHz $V_O = 3V_{RMS}, R_L = 600\Omega$		0.00004 -128		% dB

**ELECTRICAL CHARACTERISTICS:  $V_S = \pm 4V$  to  $\pm 18V$  (continued)**

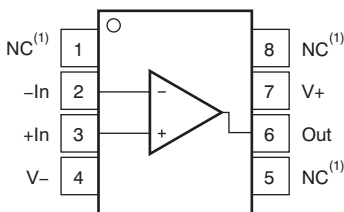
**Boldface** limits apply over the specified temperature range,  $T_A = -40^\circ C$  to  $+125^\circ C$ .

At  $T_A = +25^\circ C$ ,  $R_L = 10k\Omega$  connected to midsupply,  $V_{CM} = V_{OUT} =$  midsupply, unless otherwise noted.

PARAMETER	CONDITIONS	OPA827AI			UNIT
		MIN	TYP	MAX	
<b>OUTPUT</b>					
Voltage Output Swing	$R_L = 1k\Omega, A_{OL} > 120dB$	(V-)+3		(V+)-3	V
<b>Over Temperature</b>	$R_L = 1k\Omega, A_{OL} > 114dB$	<b>(V-)+3</b>		<b>(V+)-3</b>	<b>V</b>
Output Current	$I_{OUT}$ $ V_S - V_{OUT}  < 3V$		30		mA
Short-Circuit Current	$I_{SC}$	$\pm 55$	$\pm 65$		mA
Capacitive Load Drive	$C_{LOAD}$		See <a href="#">Typical Characteristics</a>		
Open-Loop Output Impedance	$Z_O$		See <a href="#">Typical Characteristics</a>		
<b>POWER SUPPLY</b>					
Specified Voltage	$V_S$	$\pm 4$		$\pm 18$	V
Quiescent Current (per amplifier)	$I_Q$		4.8	5.2	mA
<b>Over Temperature</b>				<b>6</b>	<b>mA</b>
<b>TEMPERATURE RANGE</b>					
Specified Range	$T_A$	-40		+125	$^\circ C$
Operating Range	$T_A$	-55		+150	$^\circ C$
Thermal Resistance	$\theta_{JA}$		150		$^\circ C/W$
SO-8, MSOP-8					

**PIN CONFIGURATION**

**D, DGK PACKAGES  
SO-8, MSOP-8  
(TOP VIEW)**



(1) NC denotes no internal connection.

**TYPICAL CHARACTERISTICS:  $V_S = \pm 18V$**

At  $T_A = +25^\circ C$ ,  $R_L = 10k\Omega$  connected to midsupply, and  $V_{CM} = V_{OUT} =$  midsupply, unless otherwise noted.

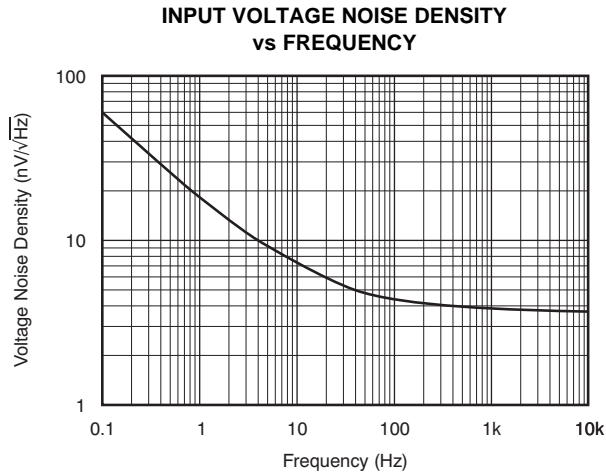


Figure 1.

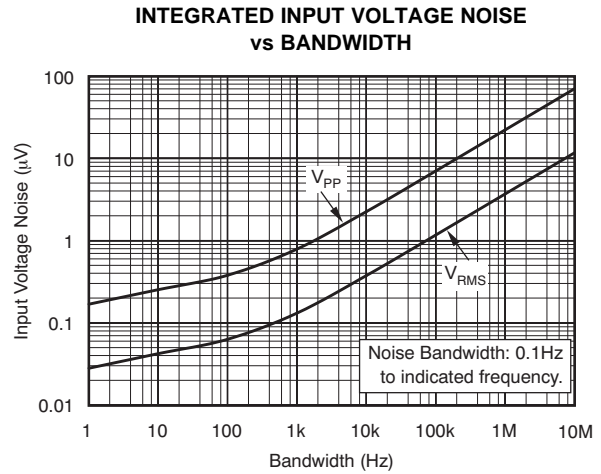


Figure 2.

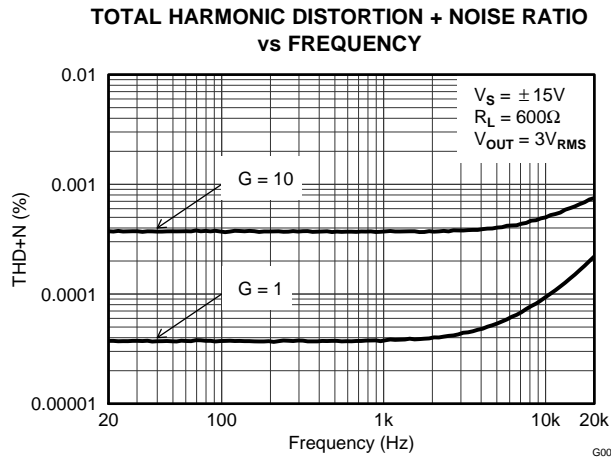


Figure 3.

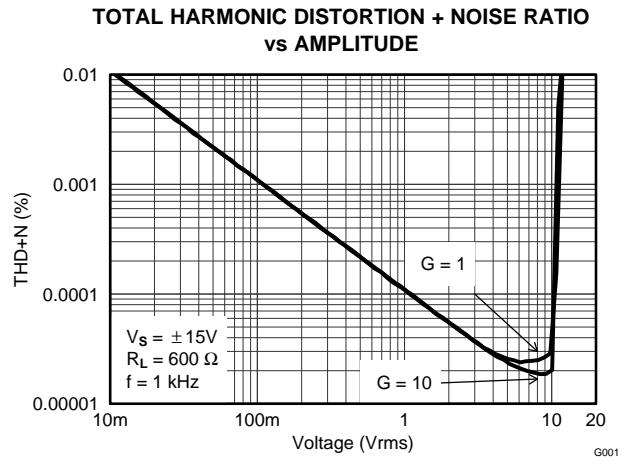


Figure 4.

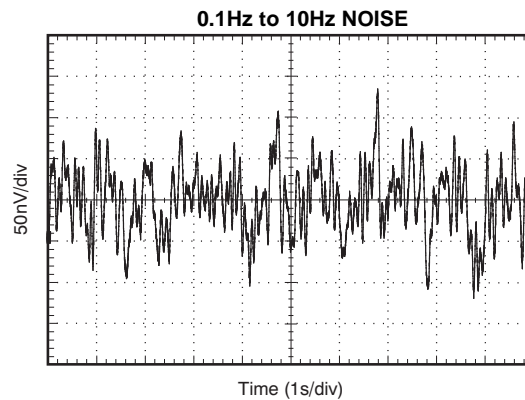


Figure 5.

**TYPICAL CHARACTERISTICS:  $V_S = \pm 18V$  (continued)**

At  $T_A = +25^\circ C$ ,  $R_L = 10k\Omega$  connected to midsupply, and  $V_{CM} = V_{OUT} =$  midsupply, unless otherwise noted.

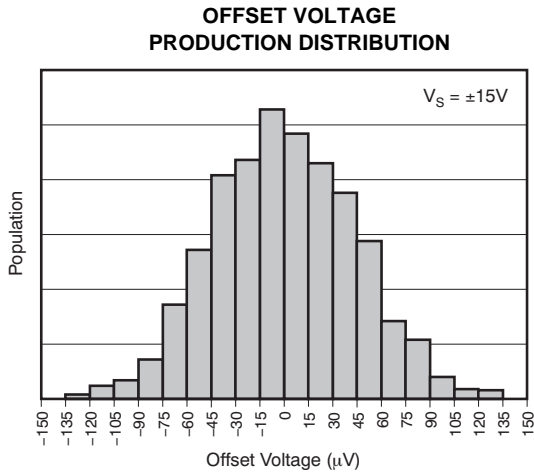


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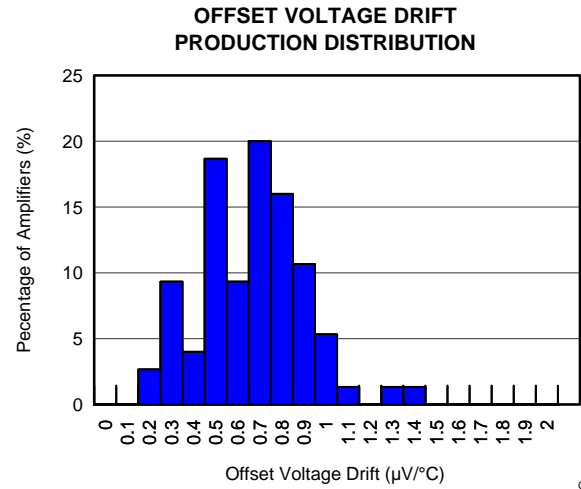


Figure 7.

G001

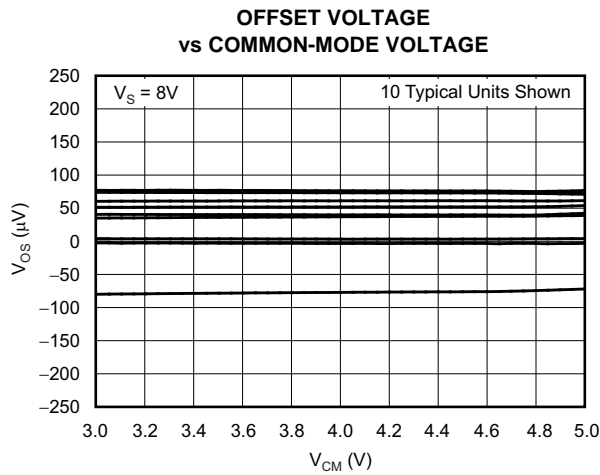


Figure 8.

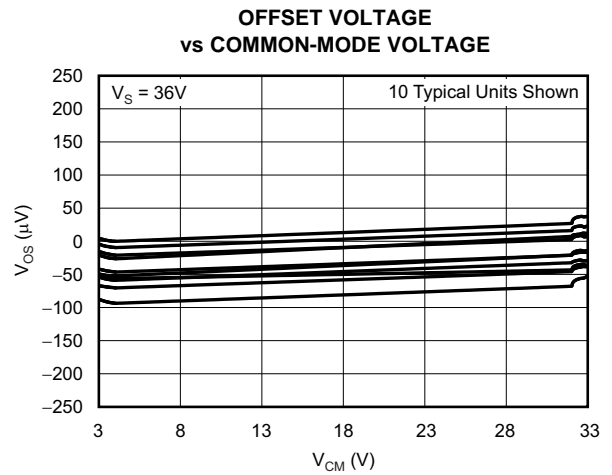


Figure 9.

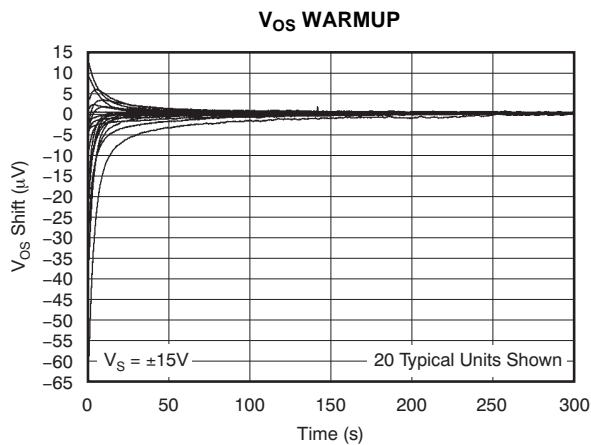


Figure 10.

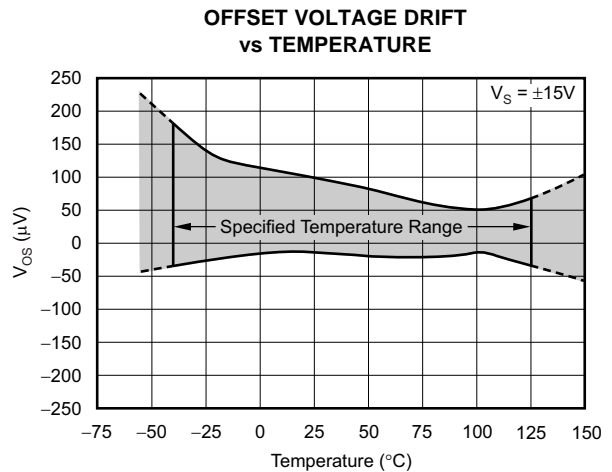


Figure 11.

**TYPICAL CHARACTERISTICS:  $V_S = \pm 18V$  (continued)**

At  $T_A = +25^\circ C$ ,  $R_L = 10k\Omega$  connected to midsupply, and  $V_{CM} = V_{OUT} =$  midsupply, unless otherwise noted.

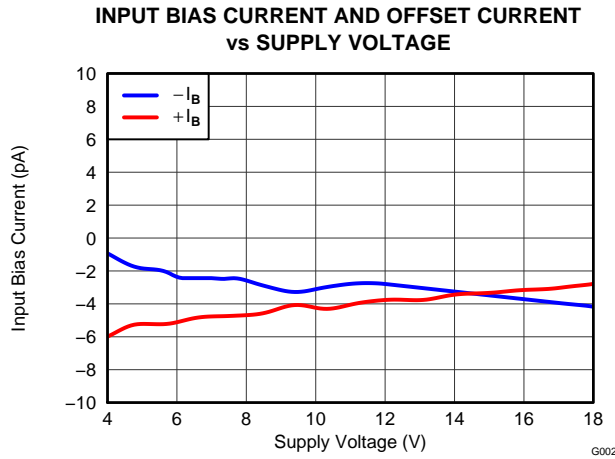


Figure 12.

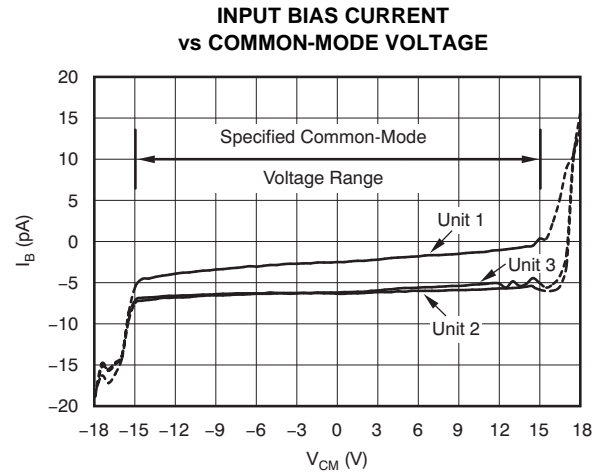


Figure 13.

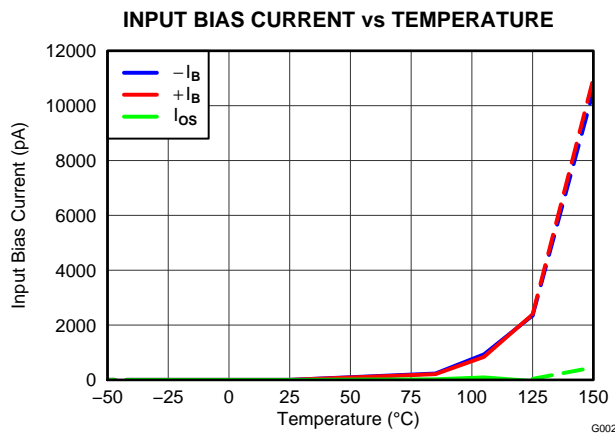


Figure 14.

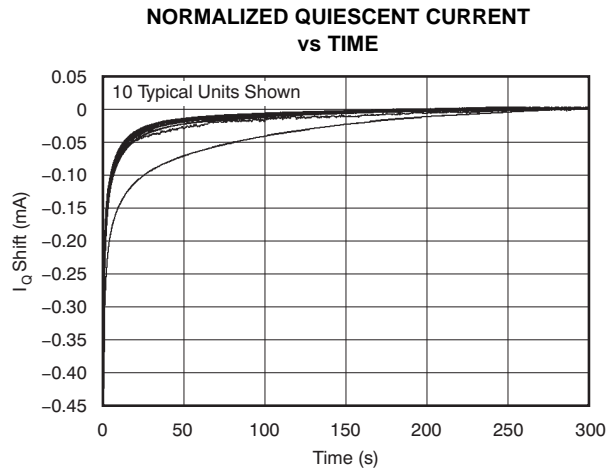


Figure 15.

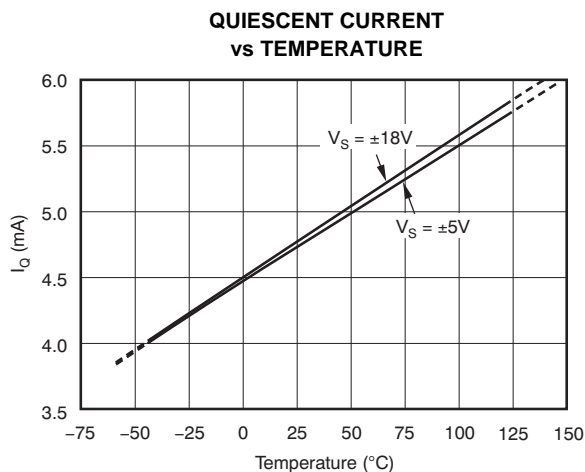


Figure 16.

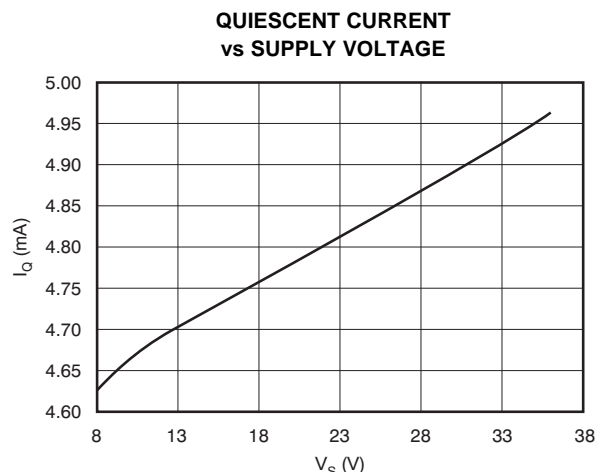


Figure 17.

**TYPICAL CHARACTERISTICS:  $V_S = \pm 18V$  (continued)**

At  $T_A = +25^\circ C$ ,  $R_L = 10k\Omega$  connected to midsupply, and  $V_{CM} = V_{OUT} =$  midsupply, unless otherwise noted.

**OUTPUT VOLTAGE SWING vs OUTPUT CURRENT**

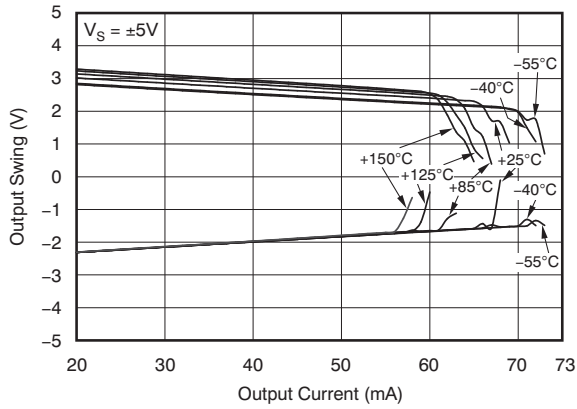


Figure 18.

**OUTPUT VOLTAGE SWING vs OUTPUT CURRENT**

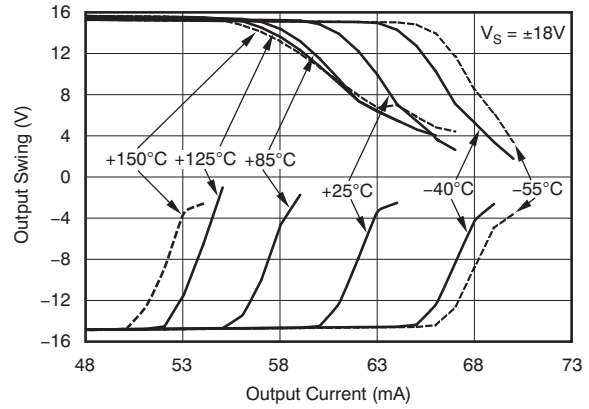


Figure 19.

**POWER-SUPPLY REJECTION RATIO vs FREQUENCY**

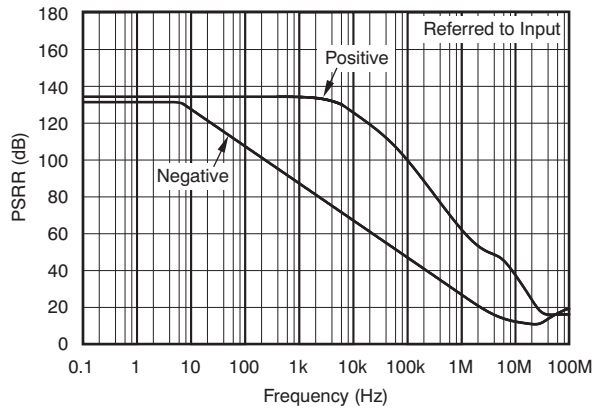


Figure 20.

**COMMON-MODE REJECTION RATIO vs FREQUENCY**

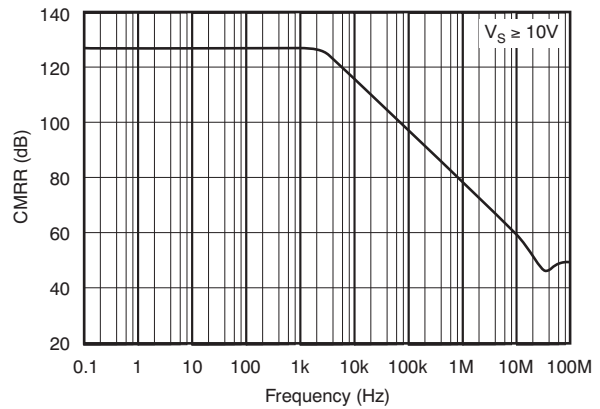


Figure 21.

**POWER-SUPPLY REJECTION RATIO vs TEMPERATURE**

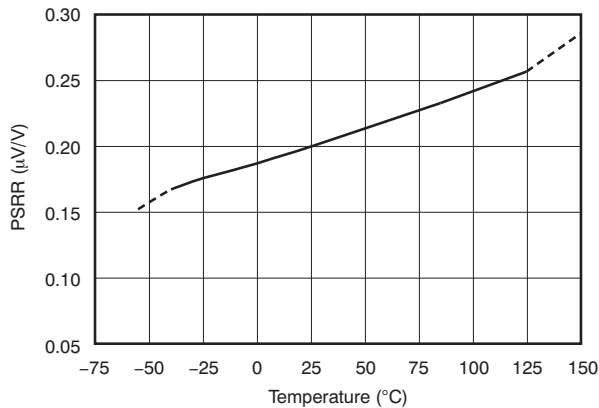


Figure 22.

**COMMON-MODE REJECTION RATIO vs TEMPERATURE**

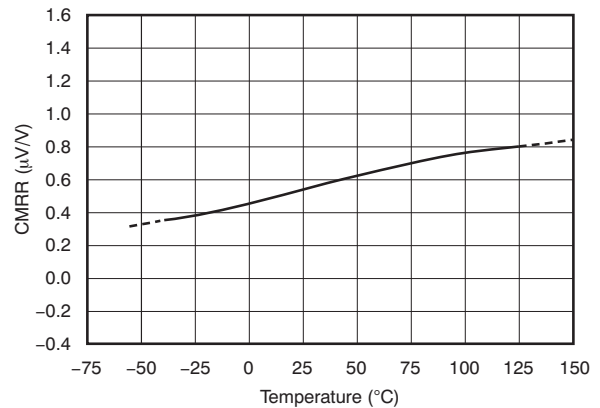


Figure 23.



**TYPICAL CHARACTERISTICS:  $V_S = \pm 18V$  (continued)**

At  $T_A = +25^\circ C$ ,  $R_L = 10k\Omega$  connected to midsupply, and  $V_{CM} = V_{OUT} =$  midsupply, unless otherwise noted.

**OPEN-LOOP GAIN AND PHASE vs FREQUENCY**

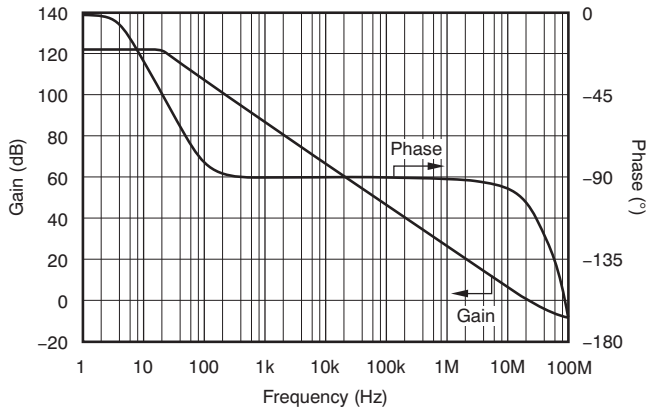


Figure 24.

**CLOSED-LOOP GAIN vs FREQUENCY**

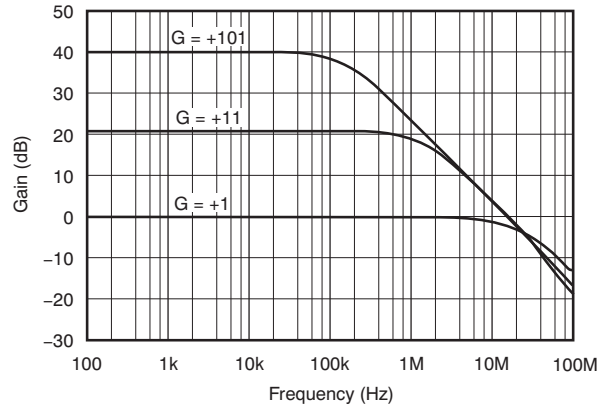


Figure 25.

**OPEN-LOOP GAIN vs TEMPERATURE**

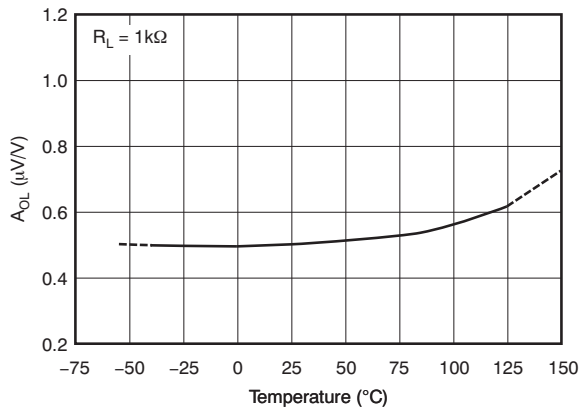


Figure 26.

**OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY**

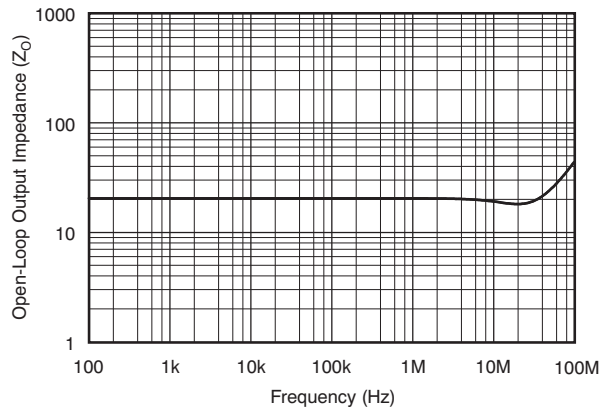


Figure 27.

**SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD**

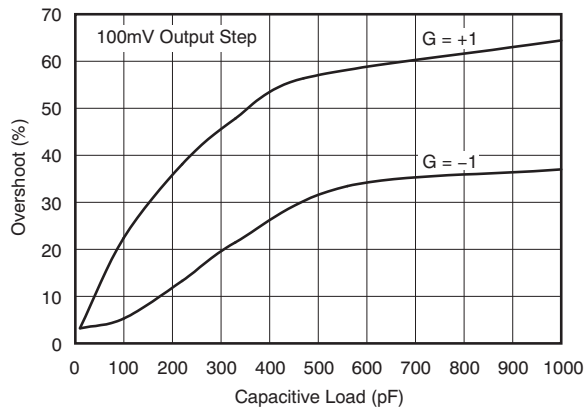


Figure 28.

**NO PHASE REVERSAL**

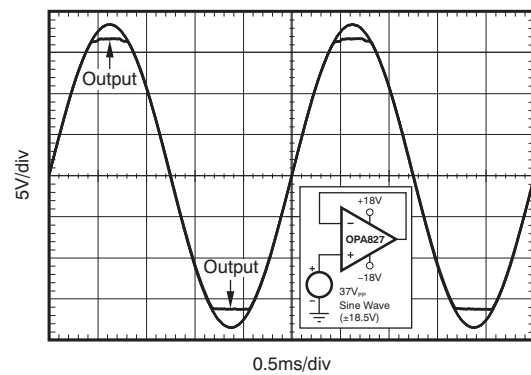
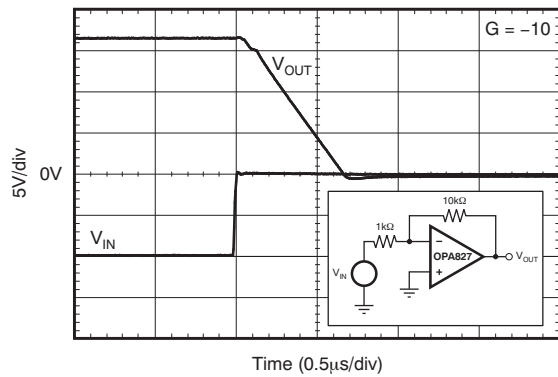


Figure 29.

**TYPICAL CHARACTERISTICS:  $V_S = \pm 18V$  (continued)**

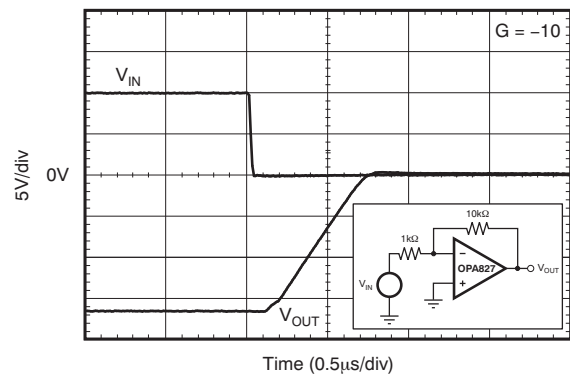
At  $T_A = +25^\circ C$ ,  $R_L = 10k\Omega$  connected to midsupply, and  $V_{CM} = V_{OUT} =$  midsupply, unless otherwise noted.

**POSITIVE OVERLOAD RECOVERY**



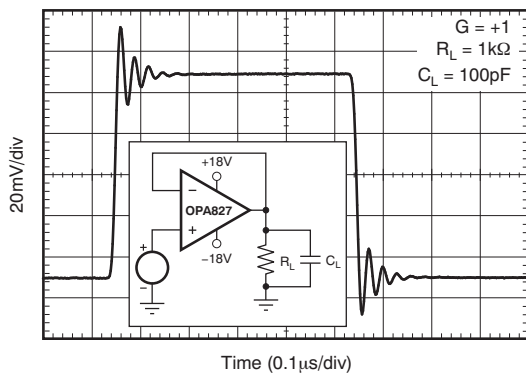
**Figure 30.**

**NEGATIVE OVERLOAD RECOVERY**



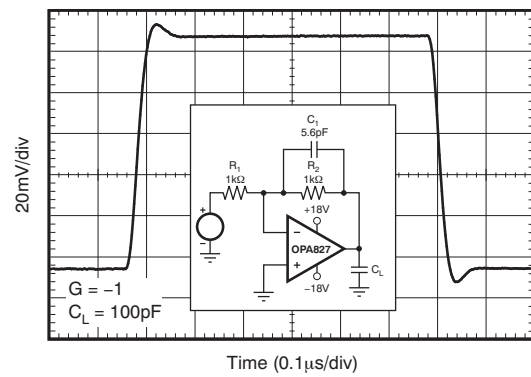
**Figure 31.**

**SMALL-SIGNAL STEP RESPONSE**



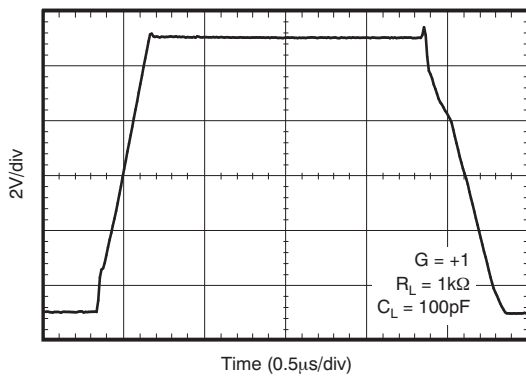
**Figure 32.**

**SMALL-SIGNAL STEP RESPONSE**



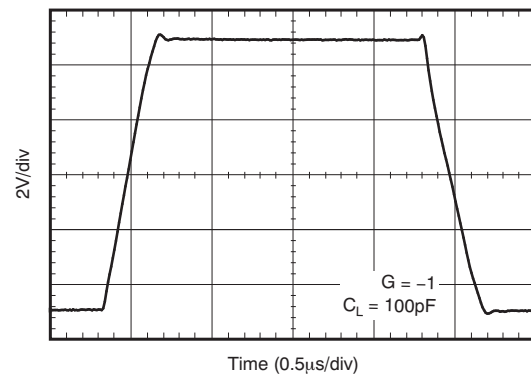
**Figure 33.**

**LARGE-SIGNAL STEP RESPONSE**



**Figure 34.**

**LARGE-SIGNAL STEP RESPONSE**



**Figure 35.**

**TYPICAL CHARACTERISTICS:  $V_S = \pm 18V$  (continued)**

At  $T_A = +25^\circ C$ ,  $R_L = 10k\Omega$  connected to midsupply, and  $V_{CM} = V_{OUT} =$  midsupply, unless otherwise noted.

**LARGE-SIGNAL POSITIVE SETTLING TIME**  
( $10V_{PP}$ ,  $C_L = 100pF$ )

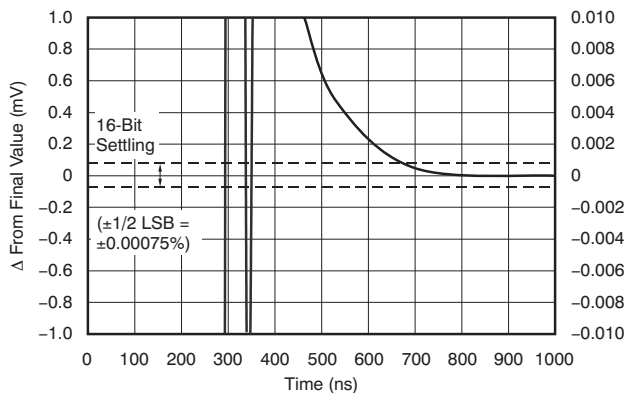


Figure 36.

**LARGE-SIGNAL POSITIVE SETTLING TIME**  
( $10V_{PP}$ ,  $C_L = 10pF$ )

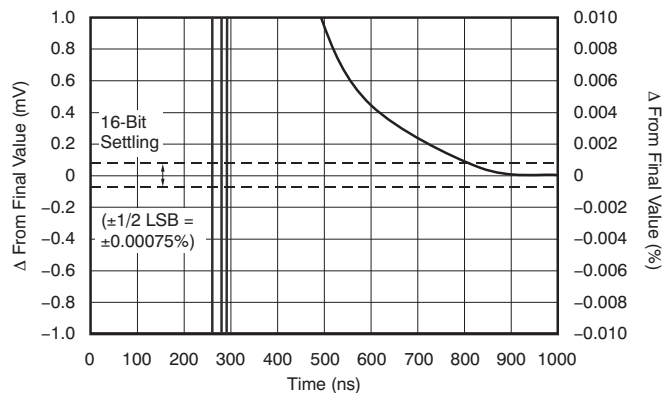


Figure 37.

**LARGE-SIGNAL NEGATIVE SETTLING TIME**  
( $10V_{PP}$ ,  $C_L = 100pF$ )

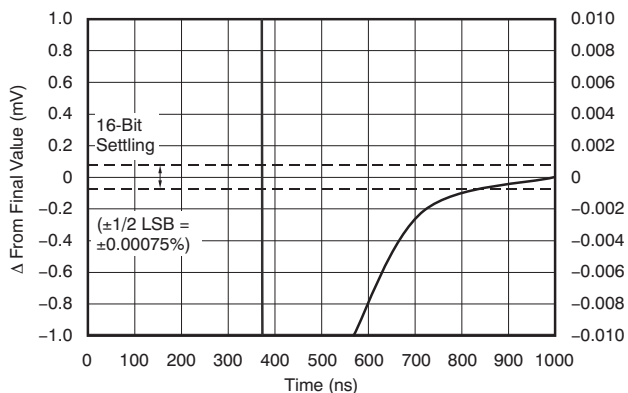


Figure 38.

**LARGE-SIGNAL NEGATIVE SETTLING TIME**  
( $10V_{PP}$ ,  $C_L = 10pF$ )

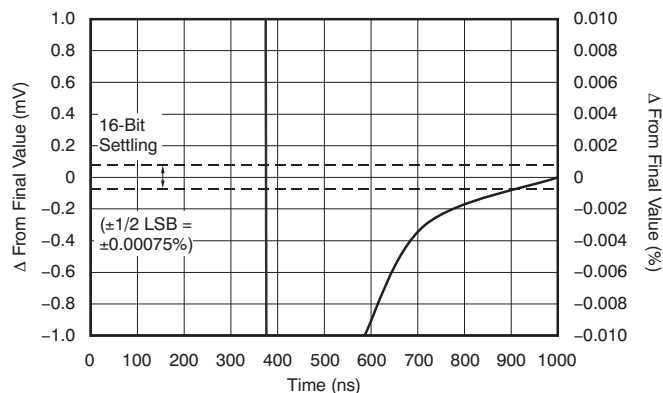


Figure 39.

**SHORT-CIRCUIT CURRENT vs TEMPERATURE**

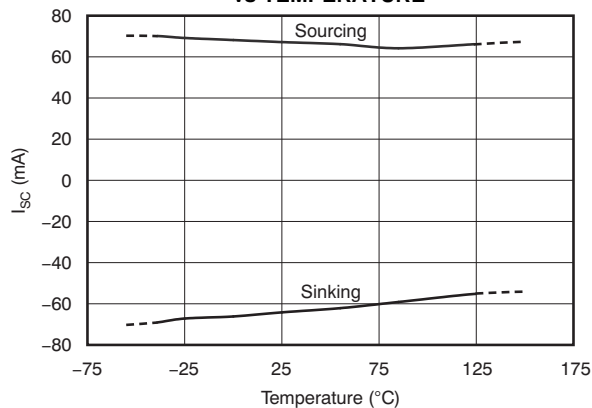


Figure 40.

## APPLICATION INFORMATION

The OPA827 is a unity-gain stable, precision operational amplifier with very low noise, input bias current, and input offset voltage. Applications with noisy or high impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1µF capacitors are adequate.

### OPERATING VOLTAGE

The OPA827 series of op amps can be used with single or dual supplies from an operating range of  $V_S = +8V (\pm 4V)$  and up to  $V_S = +36V (\pm 18V)$ . This device does not require symmetrical supplies; it only requires a minimum supply voltage of 8V. Supply voltages higher than +40V ( $\pm 20V$ ) can permanently damage the device; see the [Absolute Maximum Ratings](#) table. Key parameters are specified over the operating temperature range,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ . Key parameters that vary over the supply voltage or temperature range are shown in the [Typical Characteristics](#) section of this data sheet.

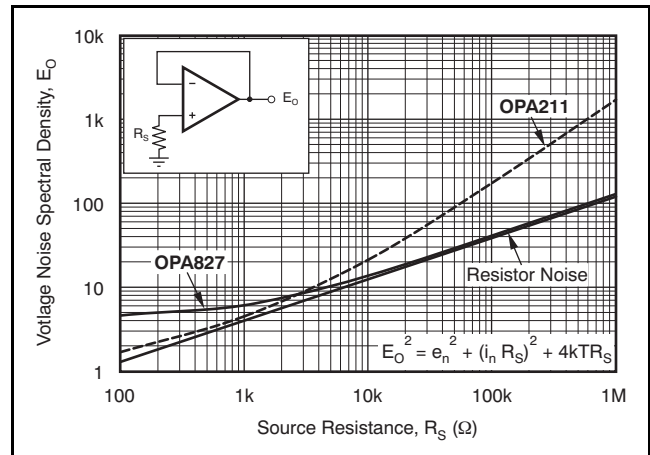
### NOISE PERFORMANCE

Figure 41 shows the total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (with no feedback resistor network and therefore no additional noise contributions). The OPA827 (GBW = 22MHz) and OPA211 (GBW = 80MHz) are both shown in this example with total circuit noise calculated. The op amp itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible, and voltage noise generally dominates. The OPA827 family has both low voltage noise and lower current noise because of the FET input of the op amp. Very low current noise allows for excellent noise performance with source impedances greater than 10kΩ. The OPA211 has lower voltage noise and higher current noise. The low voltage noise makes the OPA211 a better choice for low source impedances (less than 2kΩ). For high source impedance, current noise may dominate, and makes the OPA827 series amplifier the better choice.

The equation in Figure 41 shows the calculation of the total circuit noise, with these parameters:

- $e_n$  = voltage noise
- $i_n$  = current noise
- $R_S$  = source impedance
- $k$  = Boltzmann's constant =  $1.38 \times 10^{-23}$  J/K
- $T$  = temperature in kelvins

For more details on calculating noise, see the [Basic Noise Calculations](#) section.



**Figure 41. Noise Performance of the OPA827 and OPA211 in Unity-Gain Buffer Configuration**

### BASIC NOISE CALCULATIONS

Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases; consider the effect of source resistance on overall op amp noise performance. Total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in Figure 41. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

Figure 42 illustrates both noninverting (A) and inverting (B) op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. The current noise of the op amp reacts with the feedback resistors to create additional noise components.

The feedback resistor values can generally be chosen to make these noise sources negligible. Note that low impedance feedback resistors will load the output of the amplifier. The equations for total noise are shown for both configurations.

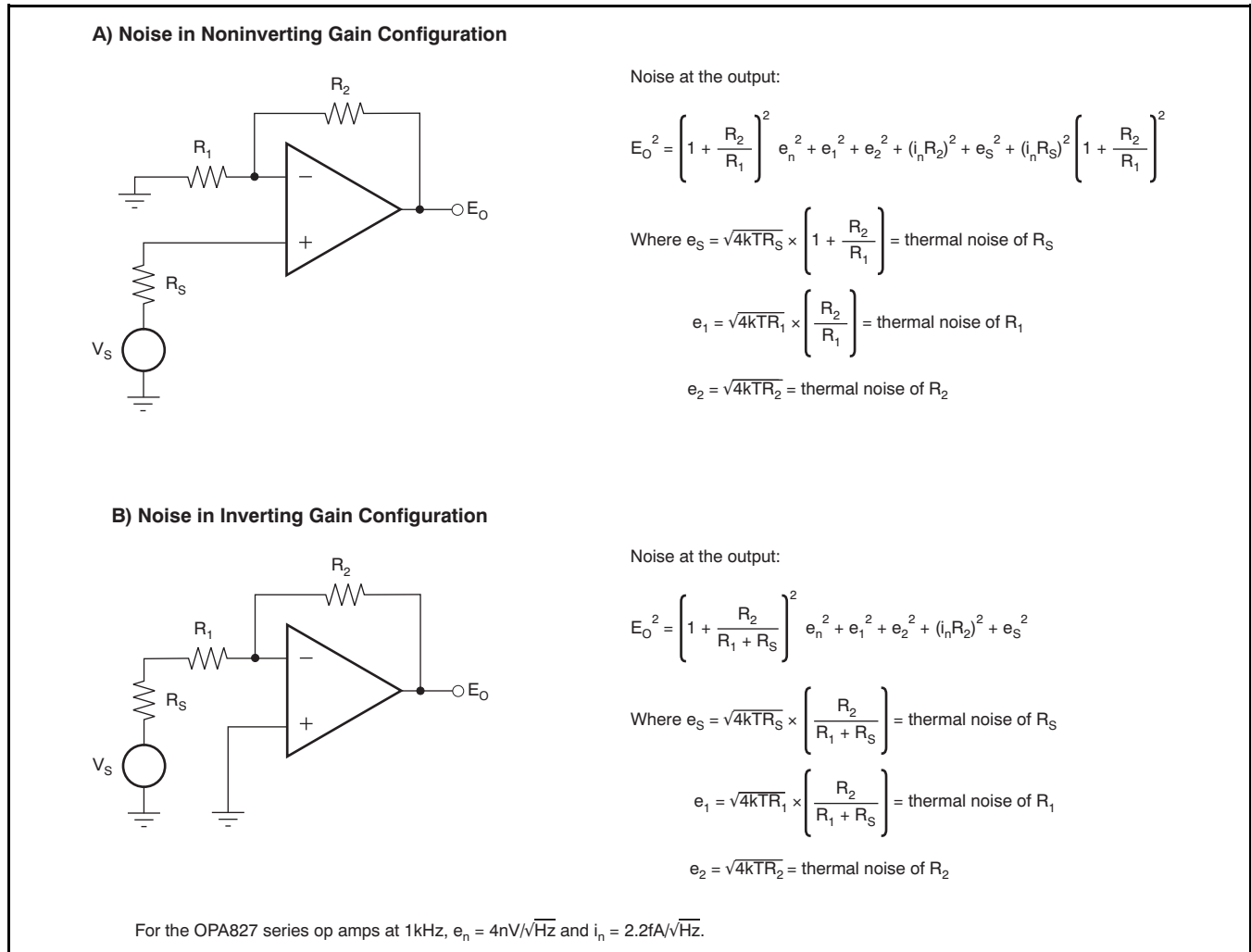


Figure 42. Noise Calculation in Gain Configurations

### TOTAL HARMONIC DISTORTION MEASUREMENTS

The OPA827 series op amps have excellent distortion characteristics. THD + Noise is below 0.0001% ( $G = +1$ ,  $V_O = 3V_{RMS}$ ) throughout the audio frequency range, 20Hz to 20kHz, with a 600Ω load (see Figure 3).

The distortion produced by the OPA827 series is below the measurement limit of many commercially available testers. However, a special test circuit (illustrated in Figure 43) can be used to extend the measurement capabilities.

Op amp distortion can be considered an internal error source that can be referred to the input. Figure 43 shows a circuit that causes the op amp distortion to be 101 times greater than that distortion normally produced by the op amp. The addition of  $R_3$  to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain

of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101, thus extending the resolution by 101. Note that the input signal and load applied to the op amp are the same as with conventional feedback without  $R_3$ . The value of  $R_3$  should be kept small to minimize its effect on the distortion measurements.

The validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with an Audio Precision System Two distortion/noise analyzer, which greatly simplifies such repetitive measurements. This measurement technique, however, can be performed with manual distortion measurement instruments.

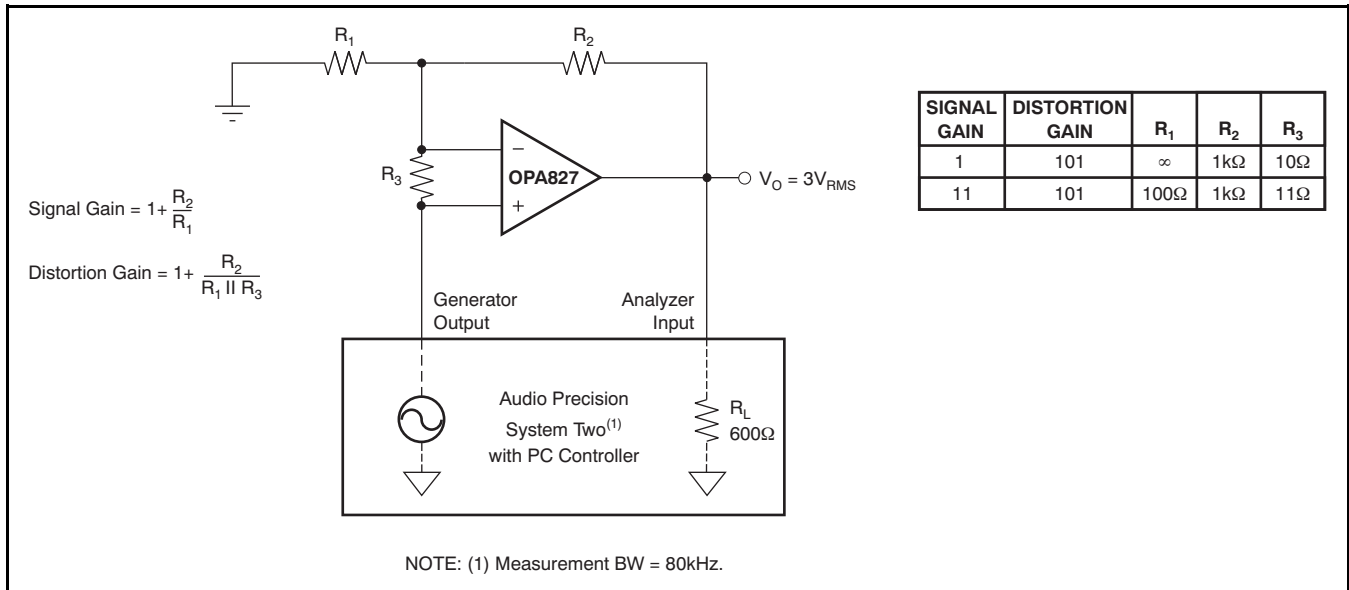


Figure 43. Distortion Test Circuit

## CAPACITIVE LOAD AND STABILITY

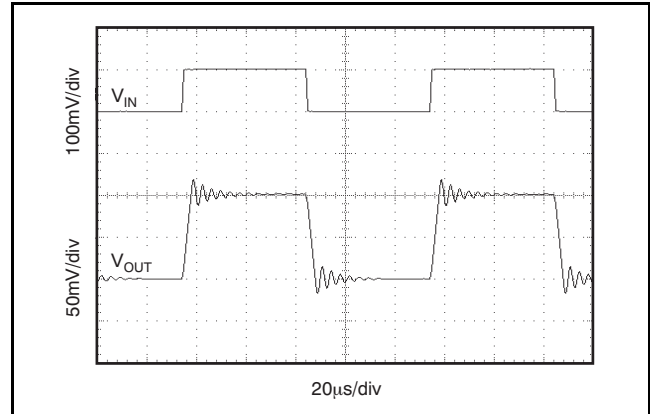
The combination of gain bandwidth product (GBW) and near constant open loop output impedance ( $Z_O$ ) over frequency gives the OPA827 the ability to drive large capacitive loads. Figure 44 shows the OPA827 connected in a buffer configuration ( $G = +1$ ) while driving a  $2.2\mu\text{F}$  ceramic capacitor (with an ESR value of approximately  $0\Omega$ ). The small overshoot and fast settling time are results of good phase margin. This feature provides superior performance compared to the competition. Figure 44 and Figure 45 were taken without any resistive load in parallel to shorten the ringing time.

In Figure 45, the OPA827 is driving a  $2.2\mu\text{F}$  tantalum capacitor. A relatively small ESR that is internal to the capacitor additionally improves phase margin and provides an output waveform with no ringing and minimal overshoot. Figure 45 shows a stable system that can be used in almost any application.

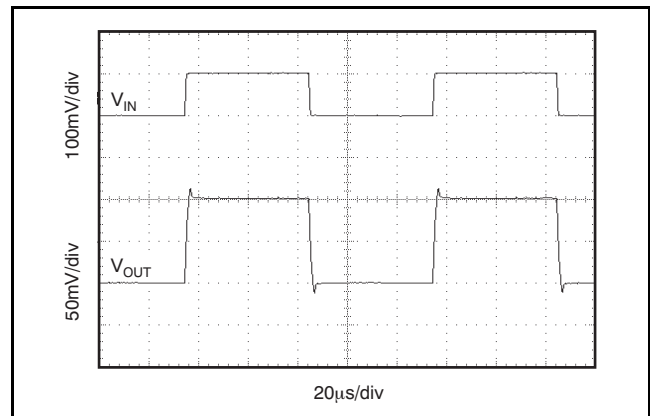
Capacitive load drive depends on the gain and overshoot requirements of the application. Capacitive loads limit the bandwidth of the amplifier. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads (see Figure 28).

## PHASE-REVERSAL PROTECTION

The OPA827 family has internal phase-reversal protection. Many FET-input op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input circuitry of the OPA827 prevents phase reversal with excessive common-mode voltage; instead, the output limits into the appropriate rail (see Figure 29).



**Figure 44. OPA827 Driving  $2.2\mu\text{F}$  Ceramic Capacitor**



**Figure 45. OPA827 Driving  $2.2\mu\text{F}$  Tantalum Capacitor**

### TRANSIMPEDANCE AMPLIFIER

The gain bandwidth, low voltage noise, and current noise of the OPA827 series make them ideal wide bandwidth transimpedance amplifiers in a photoconductive application. High transimpedance gains with feedback resistors greater than 100kΩ benefit from the low input current noise (2.2fA/Hz) of the JFET input. Low voltage noise is important because photodiode capacitance causes the effective noise gain in the circuit to increase at high frequencies. Total input capacitance of the circuit limits the overall gain bandwidth of the amplifier and is addressed below. [Figure 46](#) shows a photodiode transimpedance application.

#### Key Transimpedance Points

- The total input capacitance ( $C_{TOT}$ ) consists of the photodiode junction capacitance, and both the common-mode and differential input capacitance of the operational amplifier.
- The desired transimpedance gain,  $V_{OUT} = I_D R_F$ .
- The Unity Gain Bandwidth Product (UGBW) (22MHz for the OPA827).

With these three variables set, the feedback capacitor value ( $C_F$ ) can be calculated to ensure stability.  $C_{STRAY}$  is the parasitic capacitance of the PCB and passive components, which is approximately 0.5pF.

To ensure 45° phase margin, the minimal amount of feedback capacitance can be calculated using [Equation 1](#):

$$C_F \left( \frac{1}{4\pi R_F UGBW} \right) \left( 1 + \sqrt{1 + (8\pi C_{TOT} R_F UGBW)^2} \right) \quad (1)$$

Bandwidth ( $f_{-3dB}$ ) calculated by [Equation 2](#):

$$f_{-3dB} = \sqrt{\frac{UGBW}{2\pi R_F (C_{TOT})}} \text{ Hz} \quad (2)$$

These equations result in maximum transimpedance bandwidth. For additional information, refer to Application Bulletin [SBOA055](#), *Compensate Transimpedance Amplifiers Intuitively*, available for download at [www.ti.com](#).

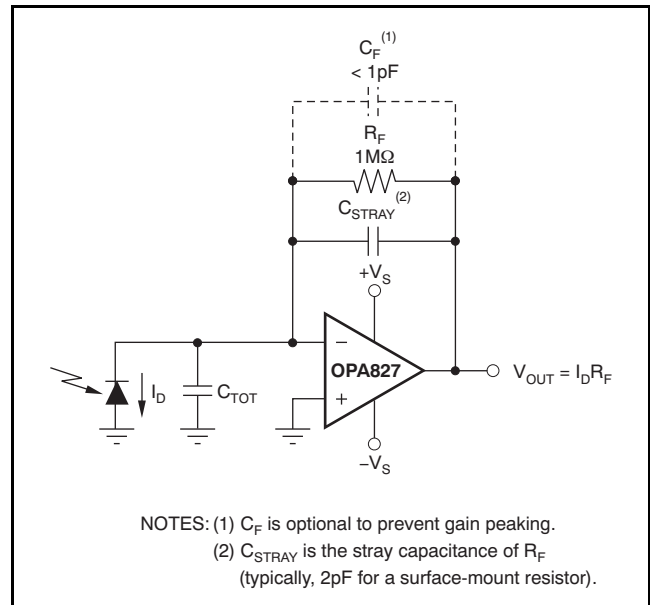


Figure 46. Transimpedance Amplifier

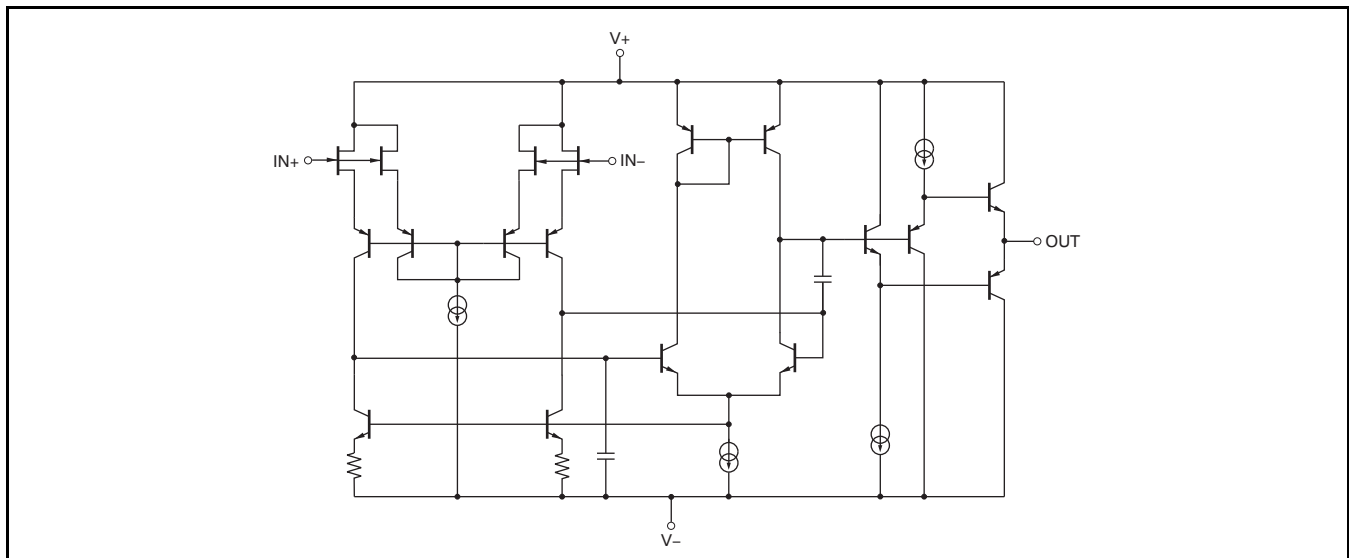


Figure 47. Equivalent Schematic (Single Channel)



## PHASE-LOCK LOOP

The OPA827 is well-suited for phase-lock loop (PLL) applications because of the low voltage offset, low noise, and wide gain bandwidth. Figure 48 illustrates an example of the OPA827 in this application. The first amplifier (OPA827) provides the loop low-pass, active filter function, while the second amplifier (OPA211) serves as a scaling amplifier. This second stage amplifies the dc error voltage to the appropriate level before it is applied to the voltage-controlled oscillator (VCO).

Operational amplifiers used in PLL applications are often required to have low voltage offset. As with other dc levels generated in the loop, a voltage offset applied to the VCO is interpreted as a phase error. An operational amplifier with inherently low voltage offset helps reduce this source of error. Also, any noise produced by the operational amplifiers modulates the voltage applied to the VCO and limits the spectral purity of the oscillator output. The VCO generates noise-related, random phase variations of its own, but this characteristic becomes worse when the input voltage source noise is included. This noise appears as random sideband energy that can limit system performance. The very low flicker noise (1/f) and current noise ( $I_n$ ) of the OPA827 help to minimize the operational amplifier contribution to the phase noise.

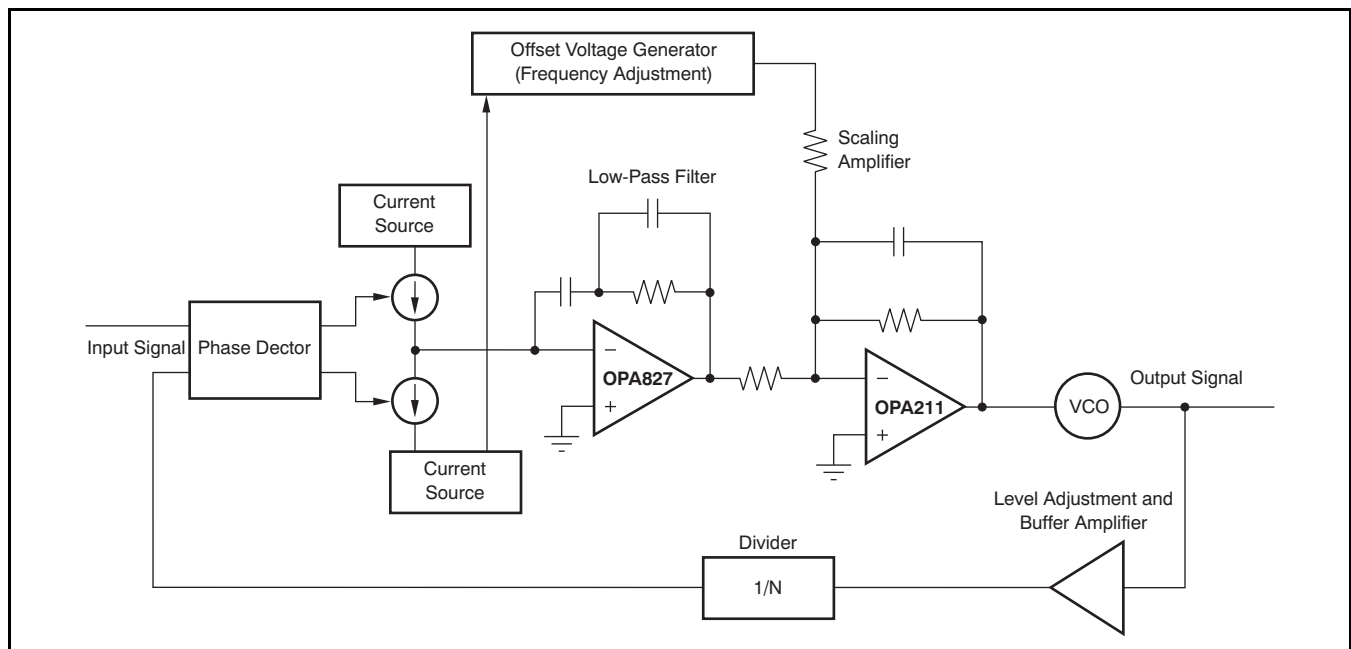


Figure 48. PLL Application

## OPA827 USED AS AN I/V CONVERTER

The OPA827 series of operation amplifiers have low current noise and offset voltage that make these devices a great choice for an I/V converter. The DAC8811 is a single channel, current output, 16-bit digital-to-analog converter (DAC). The  $I_{OUT}$  terminal of the DAC is held at a virtual GND potential by the use of the OPA827 as an external I/V converter op amp. The R-2R ladder is connected to an external reference input ( $V_{REF}$ ) that determines the DAC full-scale current. The external reference voltage can vary in a range of  $-15V$  to  $+15V$ , thus providing bipolar  $I_{OUT}$  current operation. By using the OPA827 as an external I/V converter in conjunction with the internal DAC8811  $R_{FB}$  resistor, output voltage ranges of  $-V_{REF}$  to  $+V_{REF}$  can be generated.

When using an external I/V converter and the DAC8811  $R_{FB}$  resistor, the DAC output voltage is given by Equation 3.

$$V_{OUT} = \frac{-V_{REF} \times \text{CODE}}{65536} \quad (3)$$

**NOTE:** CODE is the digital input into the DAC.

The DAC output impedance as seen looking into the  $I_{OUT}$  terminal changes versus code. The low offset voltage of the OPA827 minimizes the error propagated from the DAC.

For a current-to-voltage design (see Figure 49), the DAC8811  $I_{OUT}$  pin and the inverting node of the OPA827 should be as short as possible and adhere to good PCB layout design. For each code change on the output of the DAC, there is a step function. If the parasitic capacitance is excessive at the inverting node, then gain peaking is possible. For circuit stability, two compensation capacitors,  $C_1$  and  $C_2$  (4pF to 20pF typical) can be added to the design.

Some applications require full four-quadrant multiplying capabilities or a bipolar output swing. As shown in Figure 49, the OPA827 is added as a summing amp and has a gain of 2x that widens the output span to 20V. A four-quadrant multiplying circuit is implemented by using a 10V offset of the reference voltage to bias the OPA827.

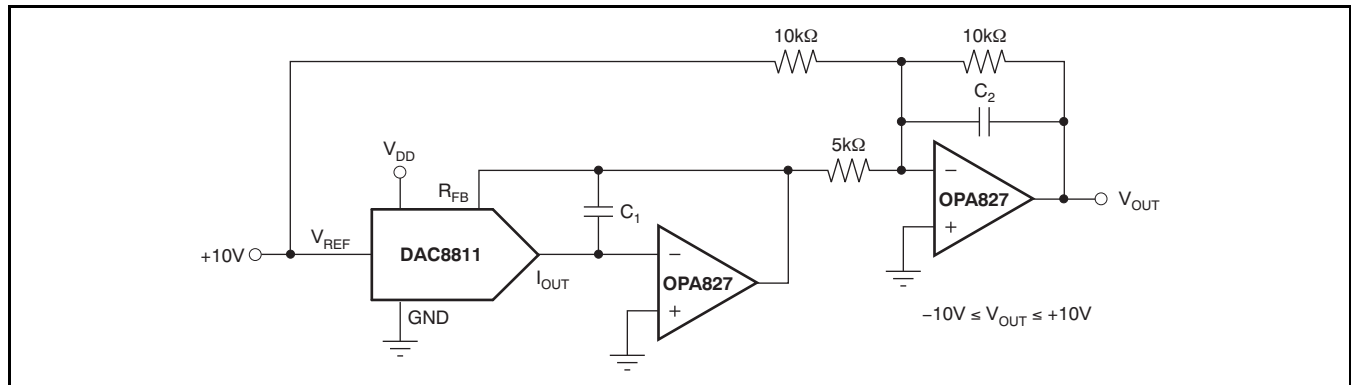


Figure 49. I/V Converter

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision G (February 2012) to Revision H</b>	<b>Page</b>
• Updated <a href="#">Figure 3</a> .....	5
• Updated <a href="#">Figure 4</a> .....	5

<b>Changes from Revision F (March 2009) to Revision G</b>	<b>Page</b>
• Changed product status from Mixed Status to Production Data .....	1
• Changed <i>Input bias current</i> and <i>Input offset drift</i> Features bullets .....	1
• Changed description of amplifier drift and bias current in first paragraph of <i>Description</i> section .....	1
• Deleted high grade (OPA827I) option and footnote 2 from Package/Ordering Information table .....	2
• Deleted high grade (OPA827I) option from Electrical Characteristics table .....	3
• Changed Offset Voltage, <i>Input Offset Voltage Drift</i> parameter typical and maximum specifications in Electrical Characteristics table .....	3
• Changed Input Bias Current section specifications in Electrical Characteristics table .....	3
• Changed -40°C to +85°C <i>Input Bias Current</i> parameter unit .....	3
• Added Frequency Response, <i>Slew Rate</i> parameter minimum specification to Electrical Characteristics table .....	3
• Deleted high grade (OPA827I) option from Electrical Characteristics table .....	4
• Added Output, <i>Short-Circuit Current</i> parameter minimum specification to Electrical Characteristics table .....	4
• Updated <a href="#">Figure 7</a> .....	6
• Updated <a href="#">Figure 8</a> .....	6
• Updated <a href="#">Figure 9</a> .....	6
• Updated <a href="#">Figure 11</a> .....	6
• Updated <a href="#">Figure 12</a> .....	7
• Updated <a href="#">Figure 14</a> .....	7

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA827AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 827 A	<a href="#">Samples</a>
OPA827AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 827 A	<a href="#">Samples</a>
OPA827AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	NSP	<a href="#">Samples</a>
OPA827AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	NSP	<a href="#">Samples</a>
OPA827AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 827 A	<a href="#">Samples</a>
OPA827AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 827 A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA827AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA827AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA827AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

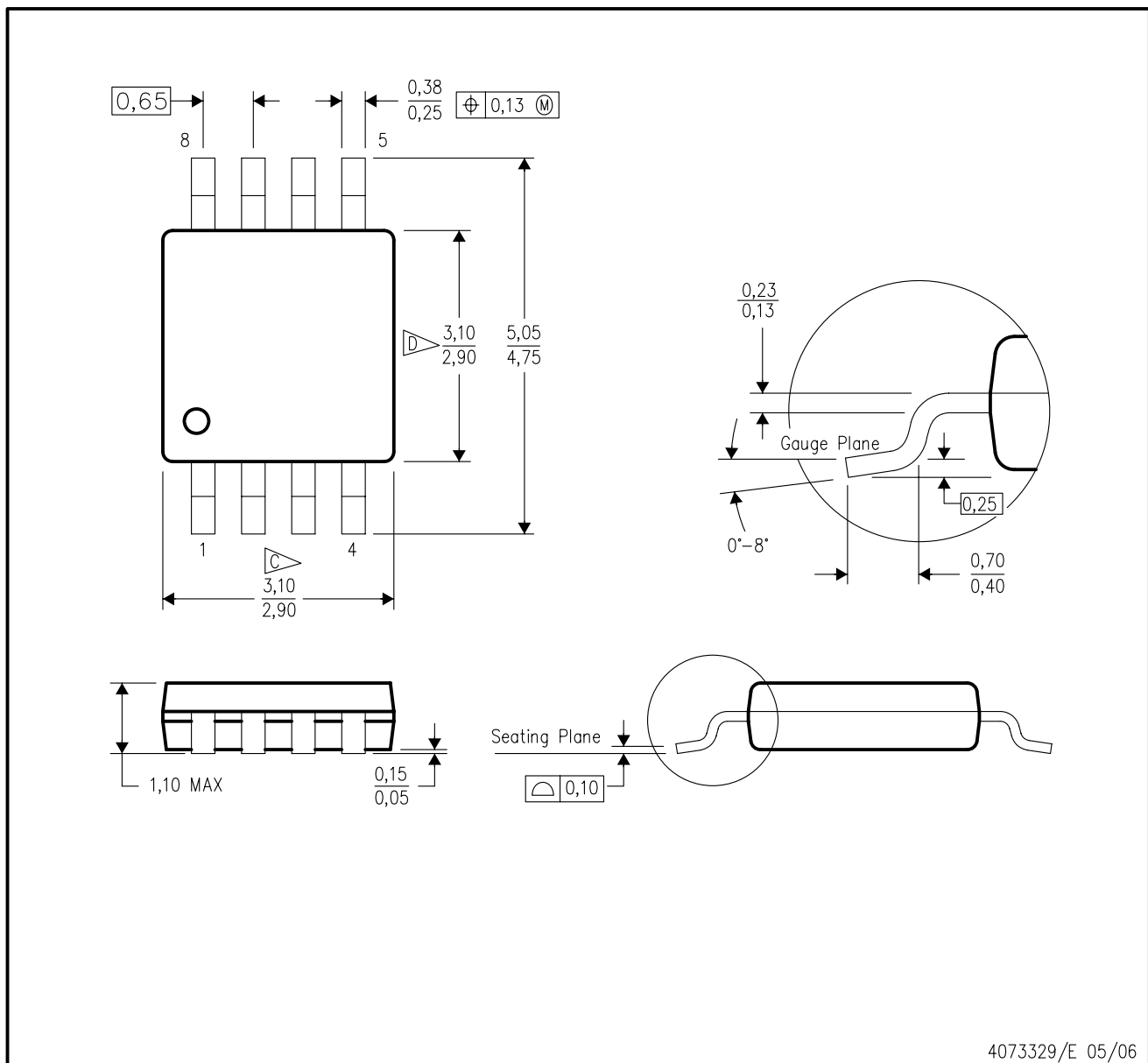
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA827AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA827AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA827AIDR	SOIC	D	8	2500	367.0	367.0	35.0

DGK (S-PDSO-G8)

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  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

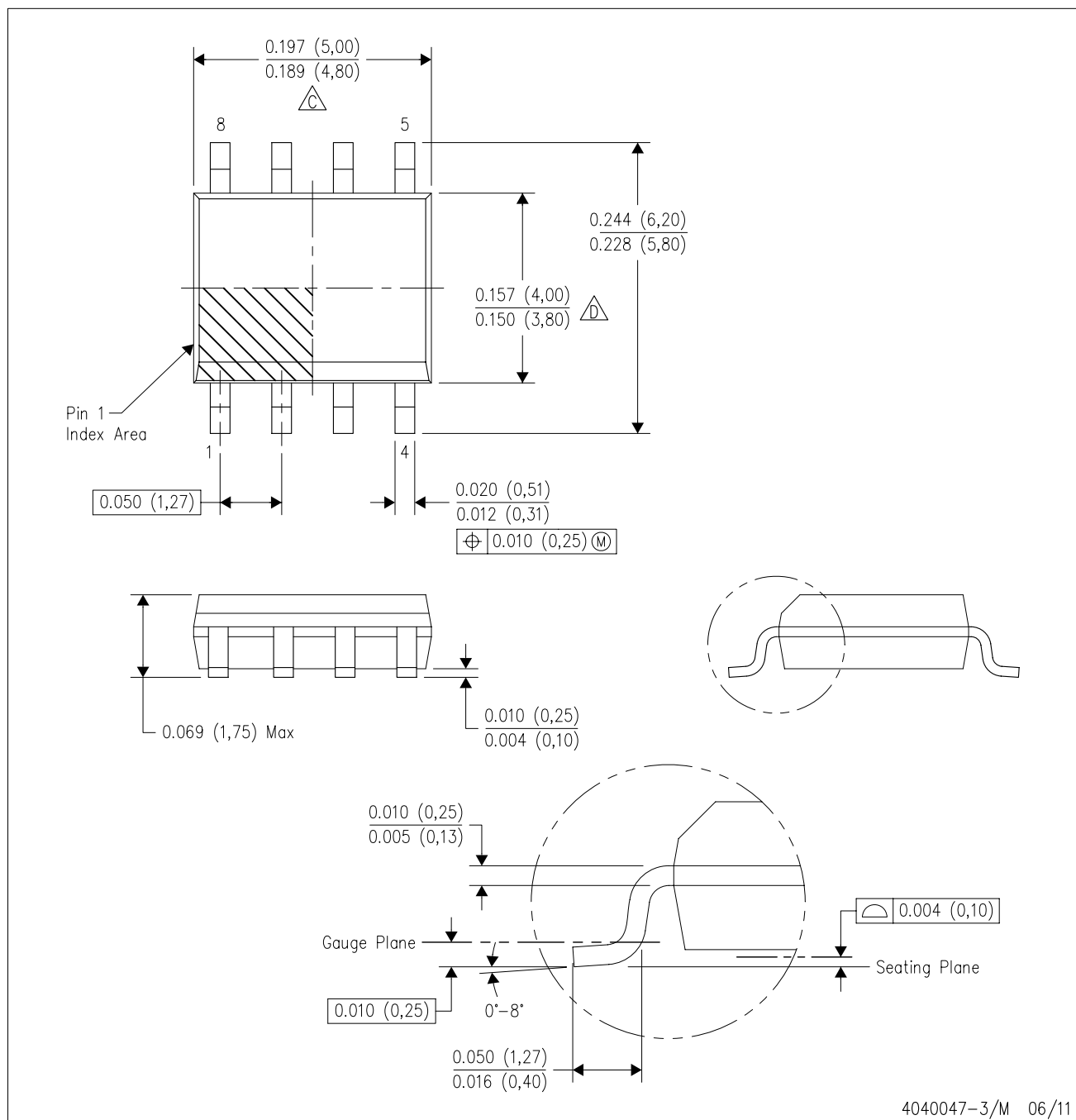






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  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

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  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

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- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
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