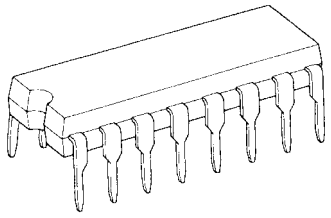
TOSHIBA Bipolar Linear Integrated Circuit Silicon Monolithic

TA8173AP

Sound Field Reproduction IC

The TA8173AP is the sound field reproduction IC developed for use on such stereo equipment as radio cassette tape recorder, multivoise TV set. etc.
This IC has made it possible to reproduce stereophonic sound with more presence by forcing difference signals of R-ch and L-ch to delay and applying these signals to R-ch and L-ch again.



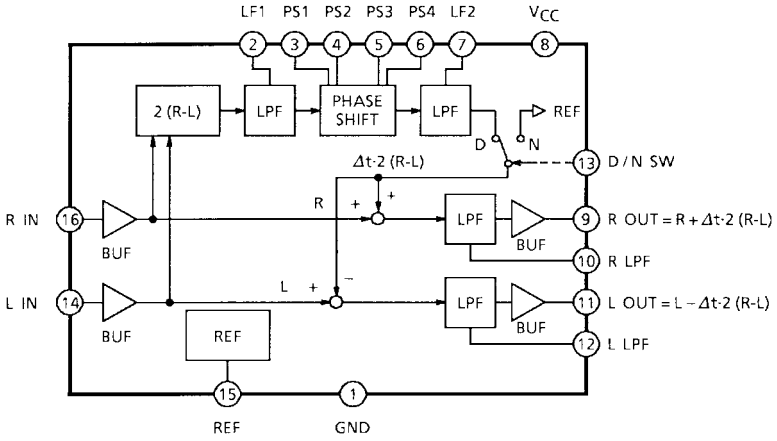
DIP16-P-300-2.54A

Weight: 1.00 g (typ.)

Features

- Built-in 4 stages of the lagging phase filter
- Built-in NORMAL/DELAY switch
- Operating supply voltage range
  : $V_{CC\ (opr)}$ = 4~12 V (Ta = 25°C)

Block Diagram



Cautions for Use

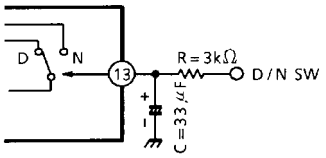
1. D/N (delay/normal) switch

The Pin 13 is the delay/normal mode selector switch. The delay mode/normal mode control voltage ranges are as follows :

V_{CC} = 5 V, Ta = 25°C

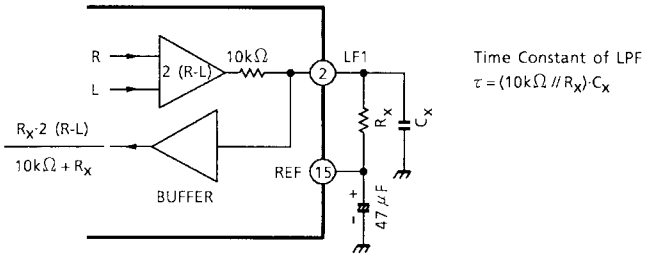
Delay mode	V_{13} = 2.0 V~V_{CC} or open
Normal mode	V_{13} = 0 V~0.2 V

If the output pop noise is generated when the delay/normal mode is Switched by pin 13, the Noise level can be reduced by smoothing current with a capacitor and resistor connected to pin 13 externally as shown in the test circuit diagram.
The recommended values are C = 33 μF and R = 3 kΩ.



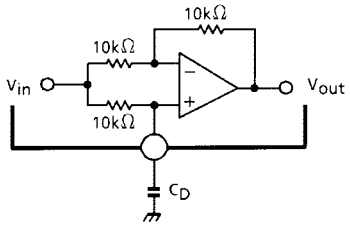
2. Delay system signal level

This IC delays phase of the difference signal (R-L) of the R (PIN 16 input) signal and L (PIN 14 input) signal and adds it to the R and L signals again. This delay system signal level has been set at 2 (R-L) in the standard circuit. However, as it is possible to reduce this signal level by externally connected parts. Set an optimum value through a listening test, etc. as shown below.
Connect a resistor from the LPF output PIN 2 or 7 to the REF PIN 15 as illustrated below. As a 10 kΩ is seen in the LPF output PIN, it is possible to attenuate the delay system signal level by dividing resistance with the external resistor R_X.
In this case as the time constant of the LPF changes when the R_X is connected, decide the LPF's time constant by (10 kΩ//R_X)·C_X again after deciding the R_X.



3. Delay system signal phase delay circuit

In the phase delay circuit of this IC, 4 stages of the block shown below are connected in series. Decide a time constant by the external C_D and total phase delay by the number of stages to be used.

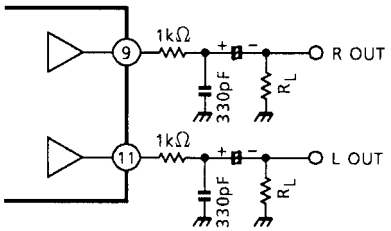


$$\frac{V_{out}}{V_{in}} = \frac{1 - j2\pi f \cdot 10k\Omega \cdot C_D}{1 + j2\pi f \cdot 10k\Omega \cdot C_D}$$

$$\phi = -2\tan^{-1}(2\pi f \cdot 10k\Omega \cdot C)$$

4. Oscillation stability

In the test circuit diagram, the capacitor (C = 330 pF) and the resistor (R = 1 kΩ) connected to the output pins 9 and 11 consist of the LPF for preventing frequency parasitic oscillation. If this LPF is not inserted in the circuit, weak oscillation of several MHz may be generated and therefore, user is advised to surely connect this LPF.



Maximum Ratings (Ta = 25°C)

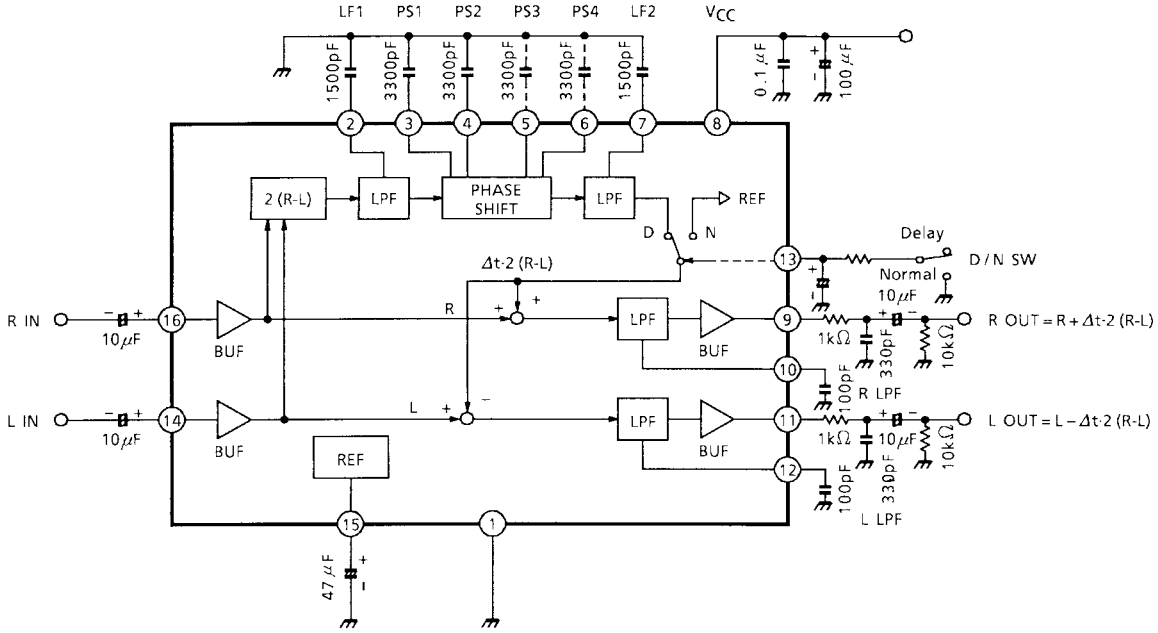
Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	14	V
Power dissipation	P_D (Note)	750	mW
Operating temperature	T_{opr}	−25~75	°C
Storage temperature	T_{stg}	−55~150	°C

Note: Derated above Ta = 25°C in the proportion of 6 mW/°C.

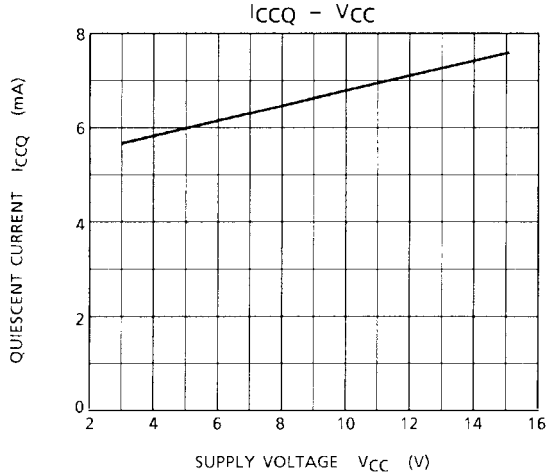
Electrical Characteristics
(unless otherwise specified, V_{CC} = 5 V, f = 1 kHz, R_L = 10 kΩ, Ta = 25°C, Normal mode)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Quiescent current	I_{CCQ}	—	V_{in} = 0	—	6	10	mA
Voltage gain 1	G_{v1}	—	—	−3	−1	1	dB
Voltage gain ratio	ΔG_v	—	—	−1	0	1	dB
Voltage gain 2	G_{v2}	—	Delay mode, f = 100 Hz	6	8	10	dB
Maximum output voltage	V_{om}	—	THD = 1%	—	1.0	—	Vrms
Total harmonic distortion	THD	—	V_{out} = 300 mVrms	—	0.02	0.2	%
Output noise voltage 1	V_{no1}	—	Normal mode, DIN AUDIO Filter IN	—	10	40	μVrms
Output noise voltage 2	V_{no2}	—	Delay mode, DIN AUDIO Filter IN	—	17	—	μVrms
Channel separation ratio	Sep.	—	V_{out} = 1 Vrms	—	−55	—	dB
Ripple rejection 1	R.R.1	—	Normal mode, f = 100 Hz, V_{ripple} = 0.316 Vrms (−10dBV)	—	−55	—	dB
Ripple rejection 2	R.R.2	—	Delay mode, f = 100 Hz, V_{ripple} = 0.316 Vrms (−10dBV)	—	−45	—	dB
Input resistance	R_{IN}	—	—	—	33	—	kΩ

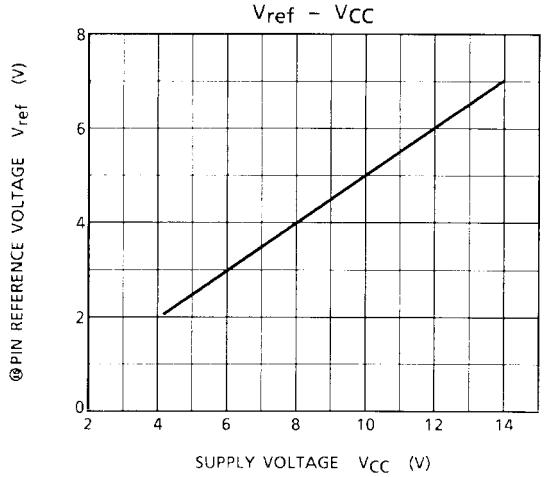
Test Circuit



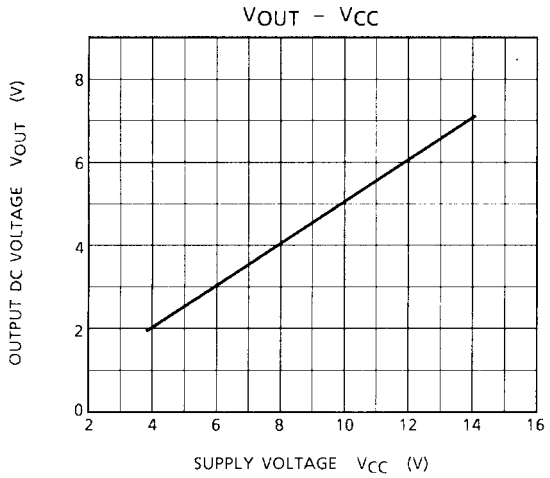
I_{CCQ} – V_{CC}



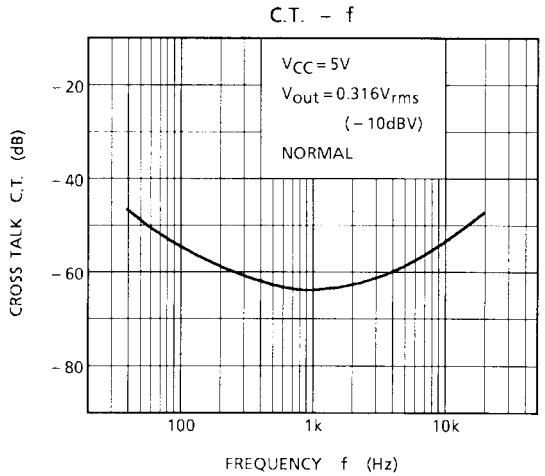
V_{ref} – V_{CC}



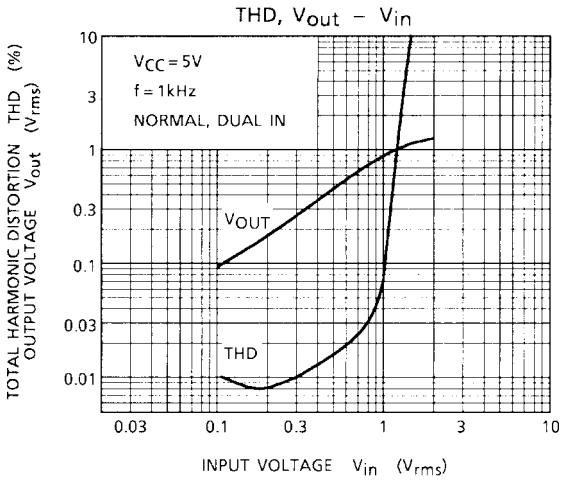
V_{OUT} – V_{CC}



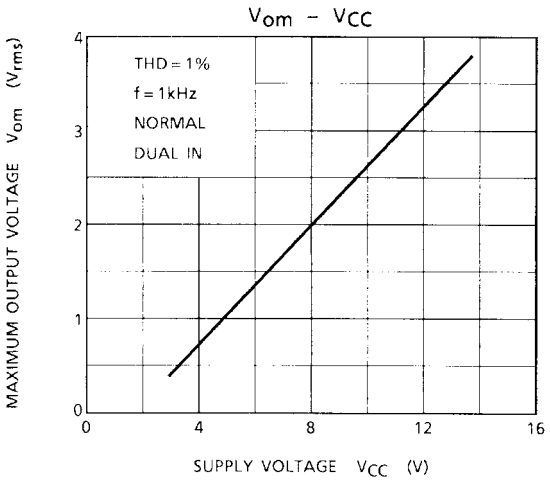
C.T. – f



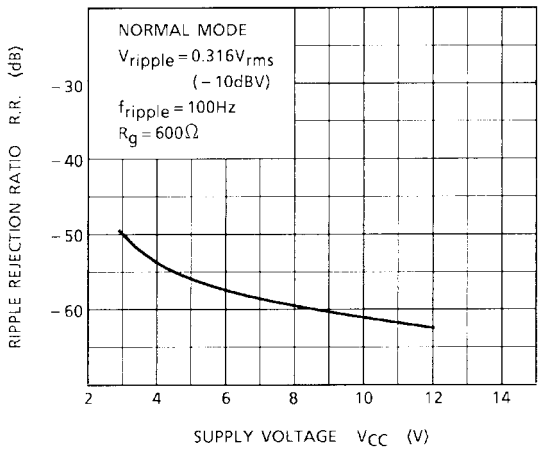
THD, V_{out} – V_{in}



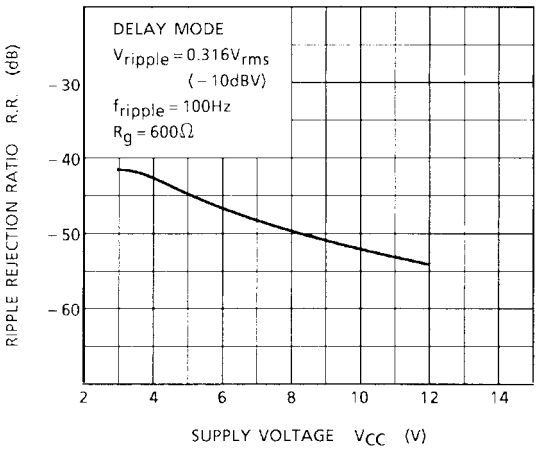
V_{om} – V_{CC}



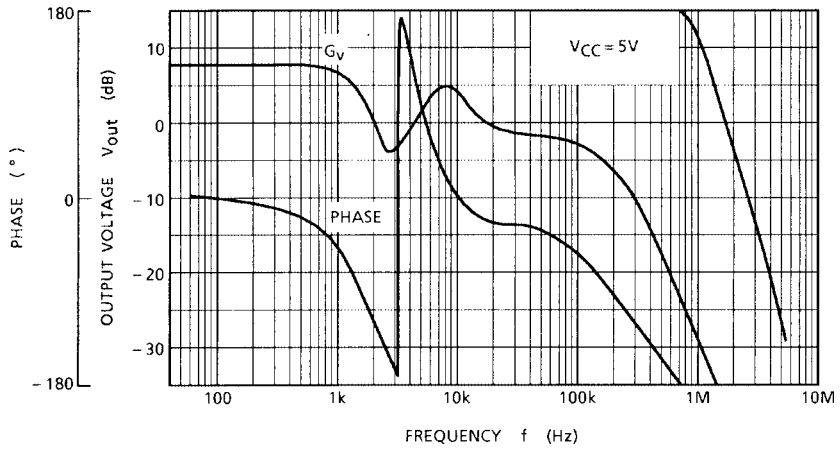
R.R. – V_{CC}



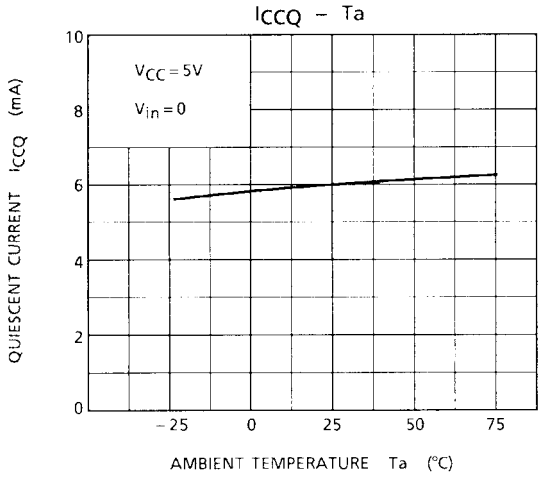
R.R. – V_{CC}



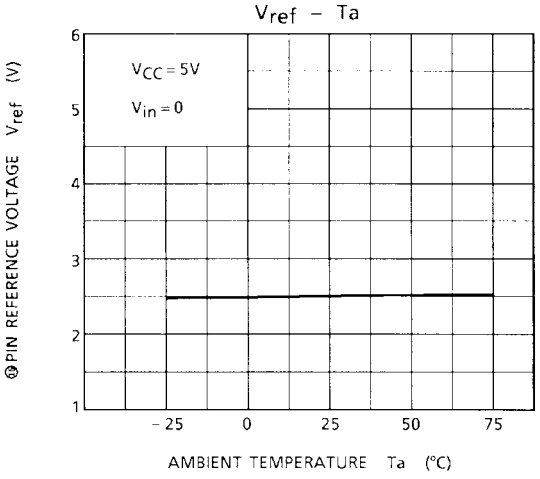
PHASE, V_{out} – f



I_{CCQ} – Ta

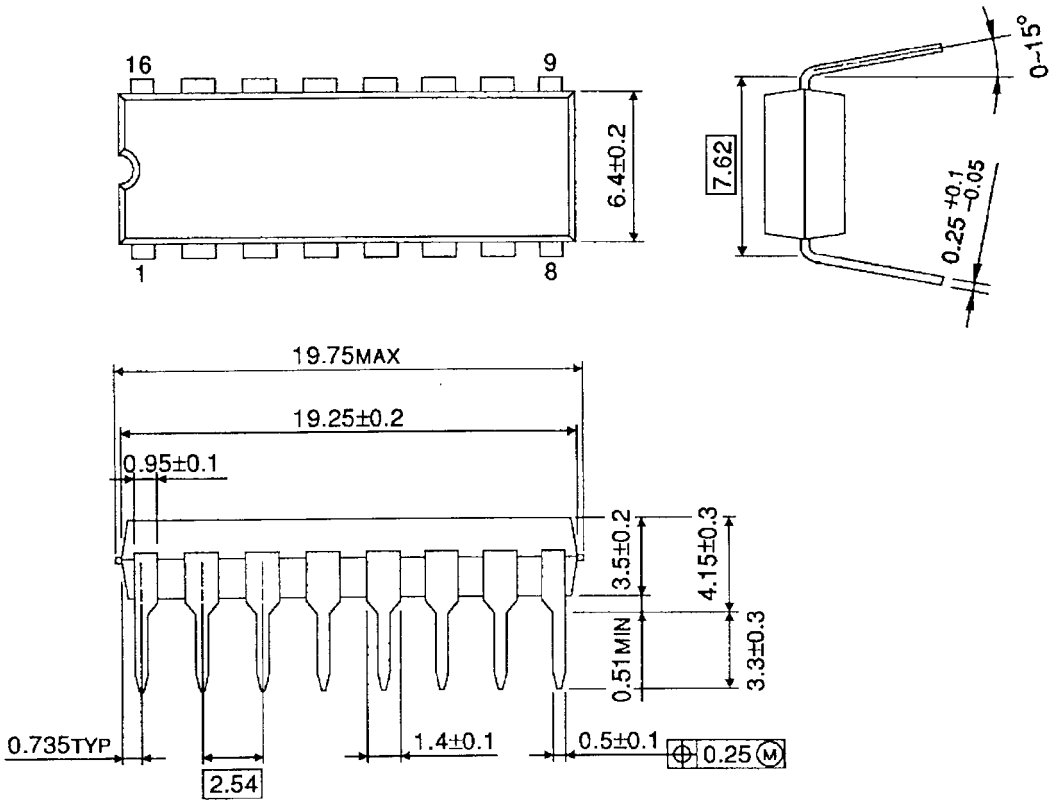


V_{ref} – Ta



Package Dimensions

DIP16-P-300-2.54A Unit : mm



Weight: 1.00 g (typ.)

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