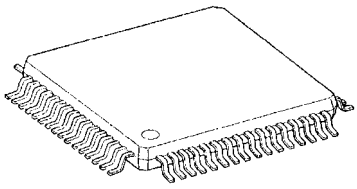
TOSHIBA Bi−CMOS INTEGRATED CIRCUIT SILICONE MONOLITHIC

TB6518F

VIDEO CAMERA CYLINDER MOTOR CONTROLLERS AND CAPSTAN MOTOR CONTROLLERS

The TB6518F is a single−chip IC for video camera cylinder motor controllers and capstan motor controllers. The cylinder section is a soft−switching pre−driver based on a 3−phase full−wave sensorless driver and 180° trapezoidal wave commutation control. The capstan section is a soft−switching pre−driver based on 3−phase full−wave drive and pseudo−sine wave commutation control.



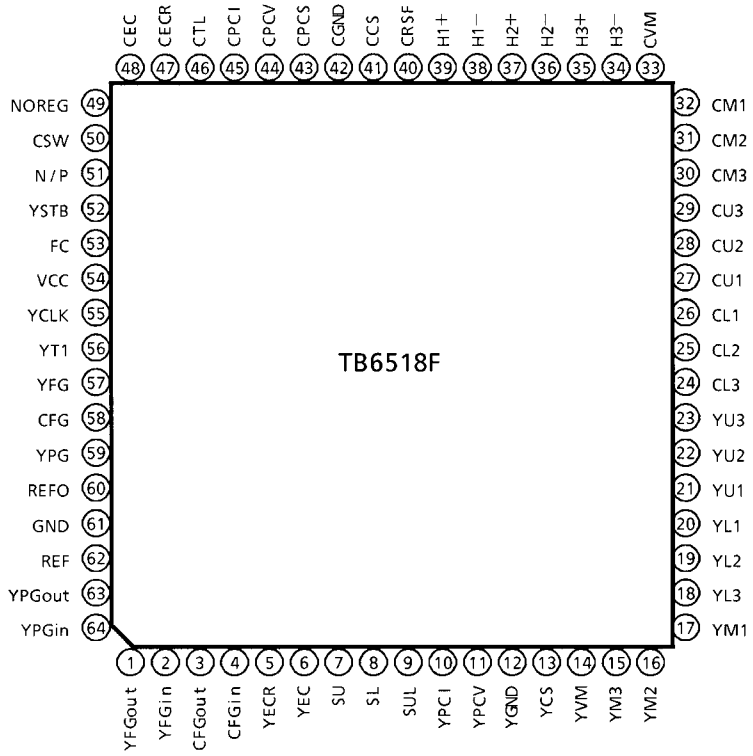
LQFP64-P-1010-0.50A

Weight: 0.34 g (Typ.)

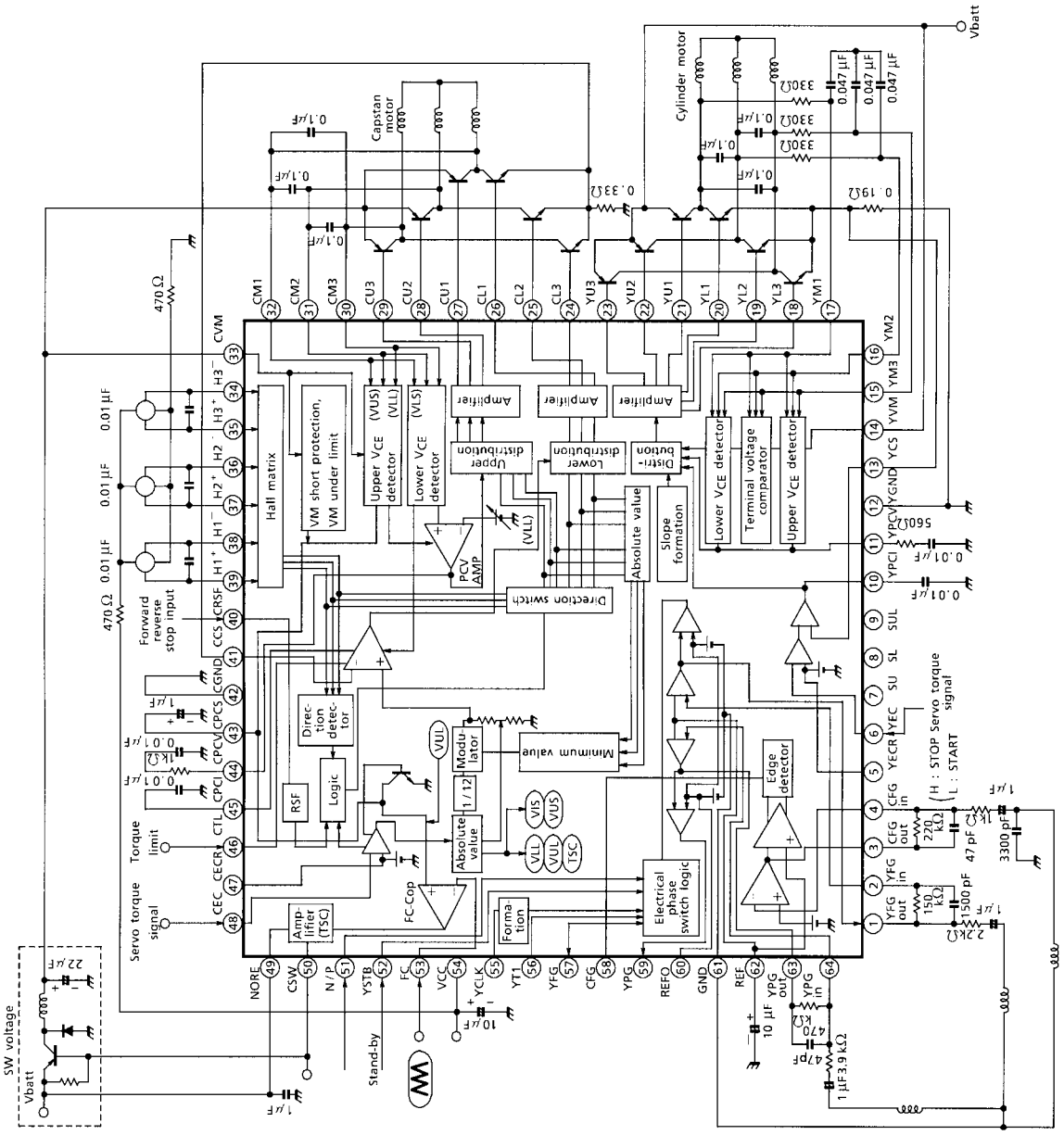
FEATURES

- Output current : 10 mA (MIN.) (At V_{CC} = 3.0 V)
- Operating voltage : V_{CC} = 2.7~5.5 V
- Motor voltage : V_M = 2.7~10 V

PIN CONNECTION



BLOCK DIAGRAM



PIN FUNCTION

PIN No.	SYMBOL	FUNCTIONAL DESCRIPTION
1	YFGout	Cylinder part FG amplifier output terminal
2	YFGin	Cylinder part FG input terminal
3	CFGout	Capstan part FG amplifier output terminal
4	CFGin	Capstan part FG input terminal
5	YECR	Cylinder part torque control reference input terminal
6	YEC	Cylinder part torque control input terminal
7	SU	Cylinder part upper slope voltage terminal
8	SL	Cylinder part lower slope voltage terminal
9	SUL	Cylinder part slope voltage terminal
10	YPCI	Cylinder part current feedback phase compensation
11	YPCV	Cylinder part voltage feedback phase compensation
12	YGND	Cylinder part ground terminal
13	YCS	Cylinder part current detection input terminal
14	YVM	Cylinder motor power voltage terminal
15	YM3	Cylinder motor coil terminal
16	YM2	”
17	YM1	”
18	YL3	Cylinder motor lower side pre−drive output terminal
19	YL2	”
20	YL1	”
21	YU1	Cylinder motor upper side pre−drive output terminal
22	YU2	”
23	YU3	”
24	CL3	Capstan motor lower side pre−driver output terminal
25	CL2	”
26	CL1	”
27	CU1	Capstan motor upper side pre−driver output terminal
28	CU2	”
29	CU3	”
30	CM3	Capstan motor coil terminal
31	CM2	”
32	CM1	”
33	CVM	Capstan motor power voltage terminal

PIN No.	SYMBOL	FUNCTIONAL DESCRIPTION
34	H3−	Capstan motor hall element input terminal
35	H3+	”
36	H2−	”
37	H2+	”
38	H1−	Capstan motor hall element input terminal
39	H1+	”
40	CRSF	Capstan part directional control input terminal
41	CCS	Capstan part current detection input terminal
42	CGND	Capstan part ground terminal
43	CPCS	Capstan part switching voltage control output
44	CPCV	Capstan part voltage feedback phase compensation
45	CPCI	Capstan part current feedback phase compensation
46	CTL	Capstan part torque limit
47	CECR	Capstan part torque control reference voltage
48	CEC	Capstan part torque control input terminal
49	NOREG	SW Tr charge removal terminal
50	CSW	Capstan part switching pre−driver output terminal
51	N / P	NTSC / PAL switch input
52	YSTB	Cylinder part stand−by switch input
53	FC	Switching comparator’s triangular−wave input terminal
54	VCC	Power voltage supply terminal for Logic
55	YCLK	Cylinder part clock input terminal
56	YT1	Cylinder part test mode switch input terminal
57	YFG	Cylinder part FG wave output terminal
58	CFG	Capstan part FG wave output terminal
59	YPG	Cylinder part PG wave output terminal
60	REFO	Amplifier part standard voltage
61	GND	FG PG part ground terminal
62	REF	FG and PG part reference voltage terminal
63	YPGout	Cylinder part PG amplifier output terminal
64	YPGin	Cylinder part PG input terminal

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V_{CC}	6	V
Motor Supply Voltage	(Note 1)	V_M	10	V
Supply Power I / O Voltage	(Note 2)	V_{SWB}	10	V
Output Terminal Voltage	(Note 3)	V_N	10	V
Input Terminal Voltage	(Note 4)	V_I	−0.3~V_{CC} + 0.3	V
Power Dissipation		P_D	0.95 (Note 5)	W
Operating Temperature		T_{opr}	−20~75	°C
Storage Temperature		T_{stg}	−55~125	°C

Note 1: Pin No. = 14, 33
Note 2: Pin No. = 50
Note 3: Pin No. = 15, 16, 17, 21, 22, 23, 27, 28, 29, 30, 31, 32
Note 4: Pin No. = 2, 4, 5, 6, 13, 41, 46, 47, 48, 49, 51, 52, 53, 55, 56, 62, 64
Note 5: Element

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = 25°C, V_{CC} = 3.0 V)

Cylinder part

No.	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
1	Supply Current (1)	$I_{CC\ (1)}$	1	Shared use of the cylinder area and capstan area during operations	—	15	20	mA
2	Supply Current (2)	$I_{CC\ (2)}$	1	During STB, during STOP (CAP)	—	6.1	12	mA
3	ECR Voltage	V_{ECR}	1		1.3	1.5	1.7	V
4	Torque Control Input Current	YI_{EC}	1	YEC = 0 V	−5	−2	—	μA
5	Torque Control Input Offset Voltage	ΔEC	2		−100	50	100	mV
6	I / O Gain	YGio	2		0.13	0.15	0.17	
7	Maximum Output Voltage	YCSmax	2	R_{YCS} = 0.27 Ω	145	168	183	mV
8	Lower Side Output Voltage (1)	$V_{L\ (1)}$	3	YCS = 54 mV	0.2	0.4	0.6	V
9	Lower Side Output Voltage (2)	$V_{L\ (2)}$	3	YECR = 1.5 V, YEC = 0 V	0.45	0.66	0.85	V
10	Upper Side Drive Current	I_U	4		—	—	−10	mA
11	Lower Side Drive Current	I_L	4		10	—	—	mA

Cylinder area

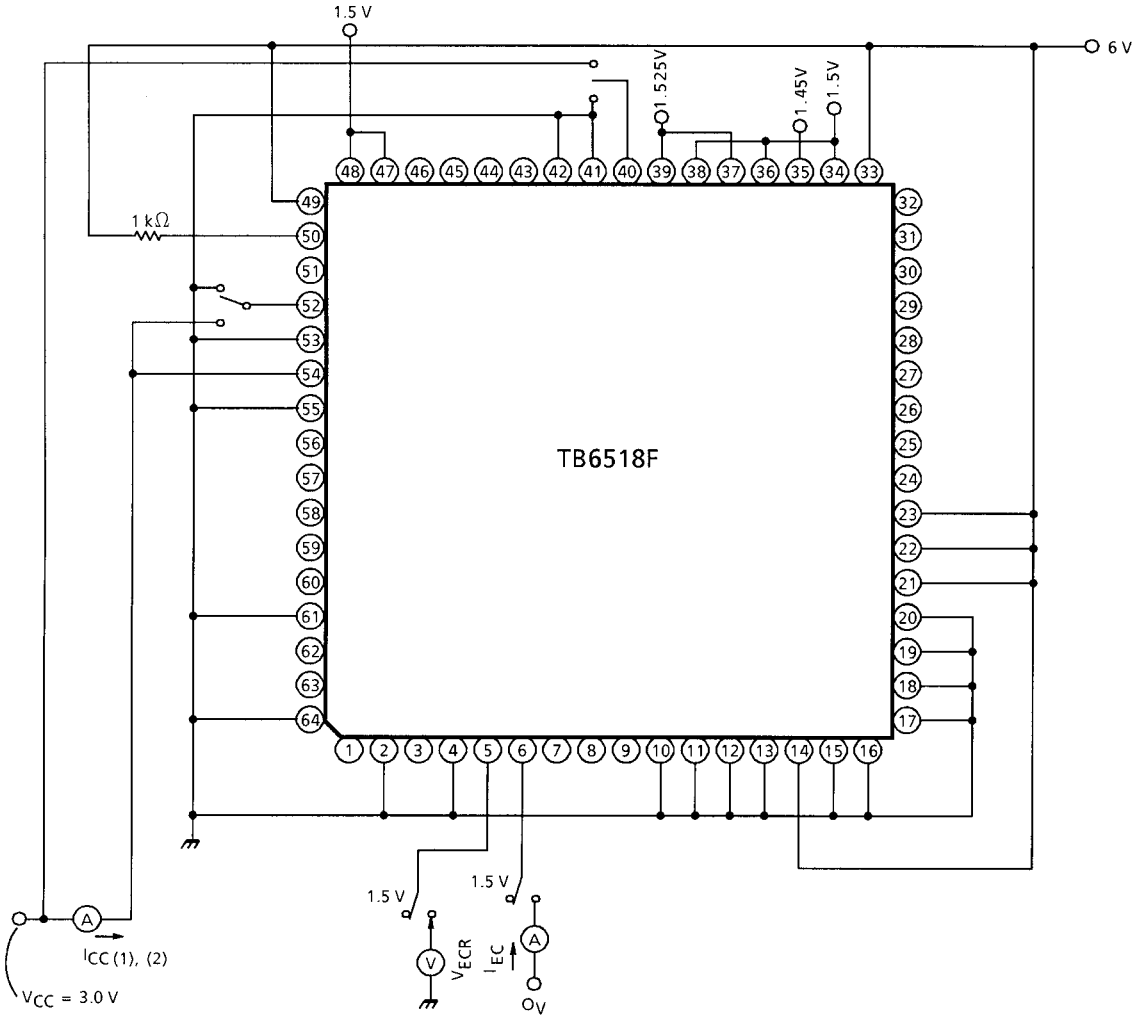
No.	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
12	FG Amplifier Gain	G_{FG}	5	V_{p-p} = 1.5 mV, f = 1 kHz	45	—	—	dB
13	YFG High Level	YFG (H)	6	I_{YFG} = −100 μA	1.0	2.8	—	V
14	YFG Low Level	YFG (L)	6	I_{YFG} = 100 μA	—	0.1	1.5	V
15	PG Amplifier Gain	G_{PG}	5	V_{p-p} = 1.5 mV, f = 1 kHz	45	—	—	dB
16	PG Amplifier Offset Voltage	ΔPGin	6		0.4	0.5	0.6	V
17	YPG High Level	YPG (H)	6	I_{YPG} = −100 μA	1.0	2.8	—	V
18	YPG Low Level	YPG (L)	6	I_{YPG} = 100 μA	—	0.1	1.5	V
19	Stand−By Voltage	STB_{on}	7		2.0	—	—	V
20	Stand−By Release Voltage	STB_{off}	7		—	—	0.8	V
21	Stand−By Input Current	I_{STB}	7	V_{STB} = 0 V	−100	−30	—	μA
22	Amplifier Reference Voltage	V_{REF}	2		1.0	1.24	1.5	V
23	Current Leak when Mains Power Off	I_{ML}	8	YVM = 6 V	—	0.1	10	μA
24	Output Idle Voltage	YCSidle	2	R_{YCS} = 0.27 Ω	—	0	5	mV
25	NTSC Operating Input Voltage	V_{NTSC}	6		2.0	—	—	V
26	PAL Operating Input Voltage	V_{PAL}	6		—	—	0.5	V
27	N / P Terminal Input Current	$I_{N / P}$	6	$V_{N / P}$ = 3 V	—	114	200	μA

Capstan area

No.	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
28	Torque Control Input Current	CI_{EC}	9	CEC = CECR = 1.5 V	−2	−1	—	μA
29	Torque Control Reference Voltage	CE_{CR}	9		1.3	1.5	1.7	V
30	Torque Control Input Voltage	CEC	10		0.2	—	2.8	V
31	Output Maximum Voltage	CCSmax	10	R_{CCS} = 0.34 Ω	0.19	0.23	—	V
32	Torque Control I / O Gain	CGio	10		0.21	0.24	0.27	
33	Output Idle Voltage	CCSidle	10		—	0	4	mV
34	Torque Control Input Offset	CECofs	10		−100	41	100	mV
35	Torque Control Dead Zone	CECdz	10		30	82	130	mV
36	Low Side V_{CE} Voltage (1)	CVLL (1)	11	CCS = 60 mV	0.22	0.29	0.50	V
37	Low Side V_{CE} Voltage (2)	CVLL (2)	11	CEC = 0 V, CTL = 1.0 V	0.40	0.54	0.80	V

No.	CHARACTERISTIC	SYMBOL	TEST CIR−CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
38	Hall Element Permissible Input Voltage	Hin	12		1.2	—	1.5	V
39	Hall Element Input Conversion Offset	Hofs	13		−8	−4.7	8	mV
40	TL−CS Offset	TLofs	14	CTL = 20 mV	6	9.5	14	mV
41	Forward Rotation Control Voltage	Vf	15		—	—	0.5	V
42	Stop Control Voltage	Vs	15		1.2	—	2.0	V
43	Reverse Rotation Control Voltage	Vr	15		2.7	—	—	V
44	Ripple Cancel Rates	R	16	CCS = 60 mV	8	11.5	18	%
45	Upper Side Drive MAX Current	CI_U	17		10	16	—	mA
46	Low Side Drive MAX Current	CI_L	17		—	−12	−8	mA
47	SW Power Voltage Input Offset	CSWofs	18		−20	13	20	mV
48	SW Power Voltage Control Output Gain	CG_{PCS}	19		6	8	10	
49	SW Power Voltage Control Output Voltage (1)	VUD (1)	19	CEC = CECR, CPCS = 1.7 V	0.28	0.34	0.6	V
50	SW Power Voltage Control Output Voltage (2)	VUD (2)	19	CEC = 0 V	—	0	0.1	V
51	SW Power Voltage Output MAX Current	CI_{SWB}	19	CEC = 0 V	10	20	—	mA
52	FG Amplifier Loop Gain	CG_{FG}	20	External 1 kΩ, 220 kΩ Input 3 mV_{p-p}, 1 kHz	43	46	—	dB
53	FG Amplifier Output Voltage High Level	CFG_H	20		2.7	3.0	—	V
54	FG Amplifier Output Voltage Low Level	CFG_L	20		—	0.0	0.5	V
55	V_M Under Limit	CV_{ML}	21		1.13	1.45	1.88	V
56	V_M Short Protection	CV_{MS}	21		0.26	0.49	1.00	V
57	SW Output Enforced ONEC Voltage	SWEC	19		—	—	0.6	V
58	NOREG Terminal Current	I_{REG}	18		—	0	2.0	μA

TEST CIRCUIT 1. $I_{CC\ (1)}$, $I_{CC\ (2)}$, V_{ECR}, YI_{EC}



No. 1 $I_{CC\ (1)}$

Set YSTB = 0 V, YEC = 0 V, YECR = 1.5 V, CEC = 0 V, CECR = 1.5 V and CRSF = 0 V and then measure the current flowing into the V_{CC} terminal.

No. 2 $I_{CC\ (2)}$

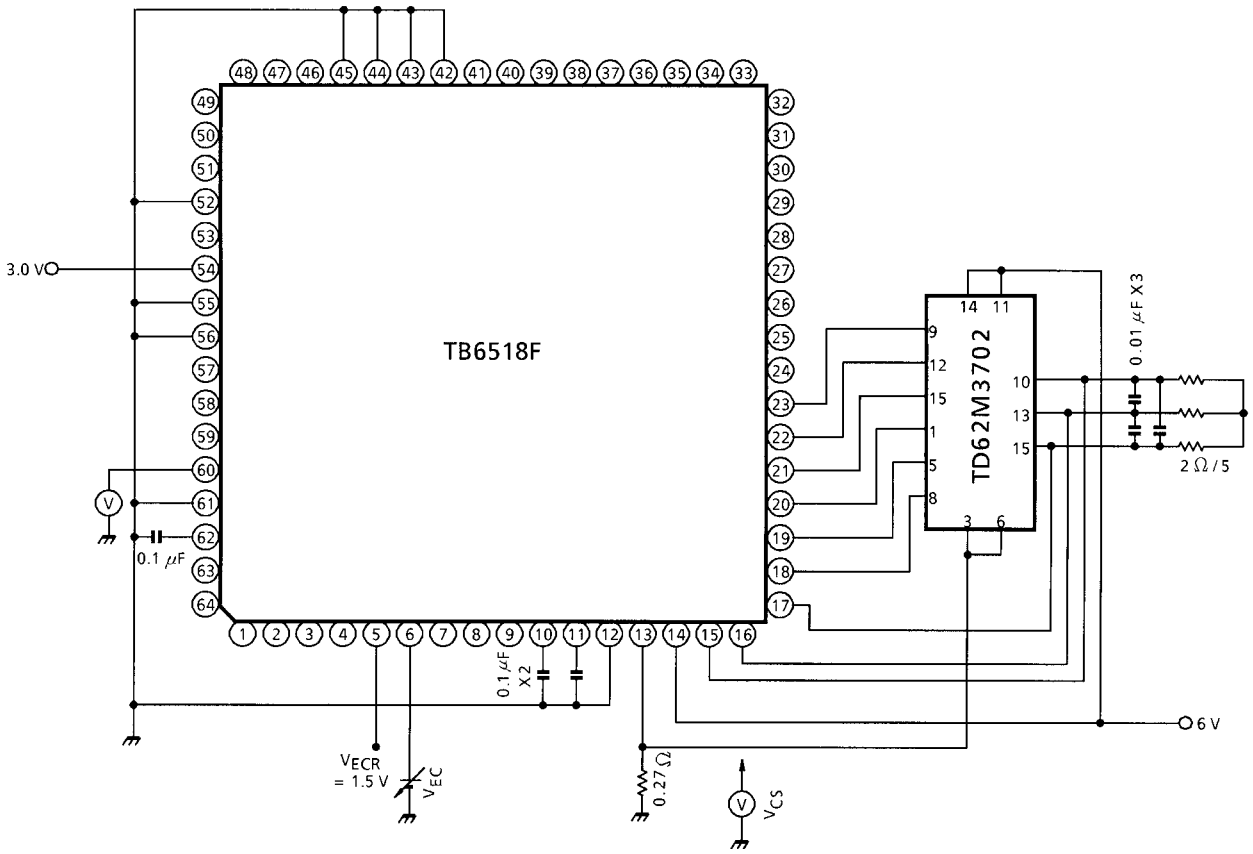
Set YSTB = 3 V, YEC = YECR = 1.5 V, CEC = CECR = 1.5 V and CRSF = OPEN and then measure the current flowing into the V_{CC} terminal.

No. 3 V_{ECR}

Measure the potential of pin (5).

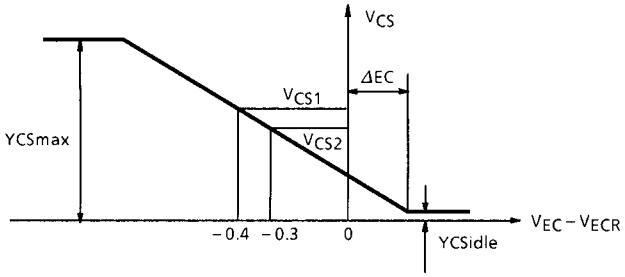
No. 4 YI_{EC}

TEST CIRCUIT 2. ΔEC, YGio, YCSmax, YCSidle, V_{REF}



No. 5 ΔEC, No. 6 YGio, No. 7 YCSmax, No. 24 YCSidle

Set YECR = 1.5 V, change YEC from 0 V to 3 V and then measure the potential of pin (13).



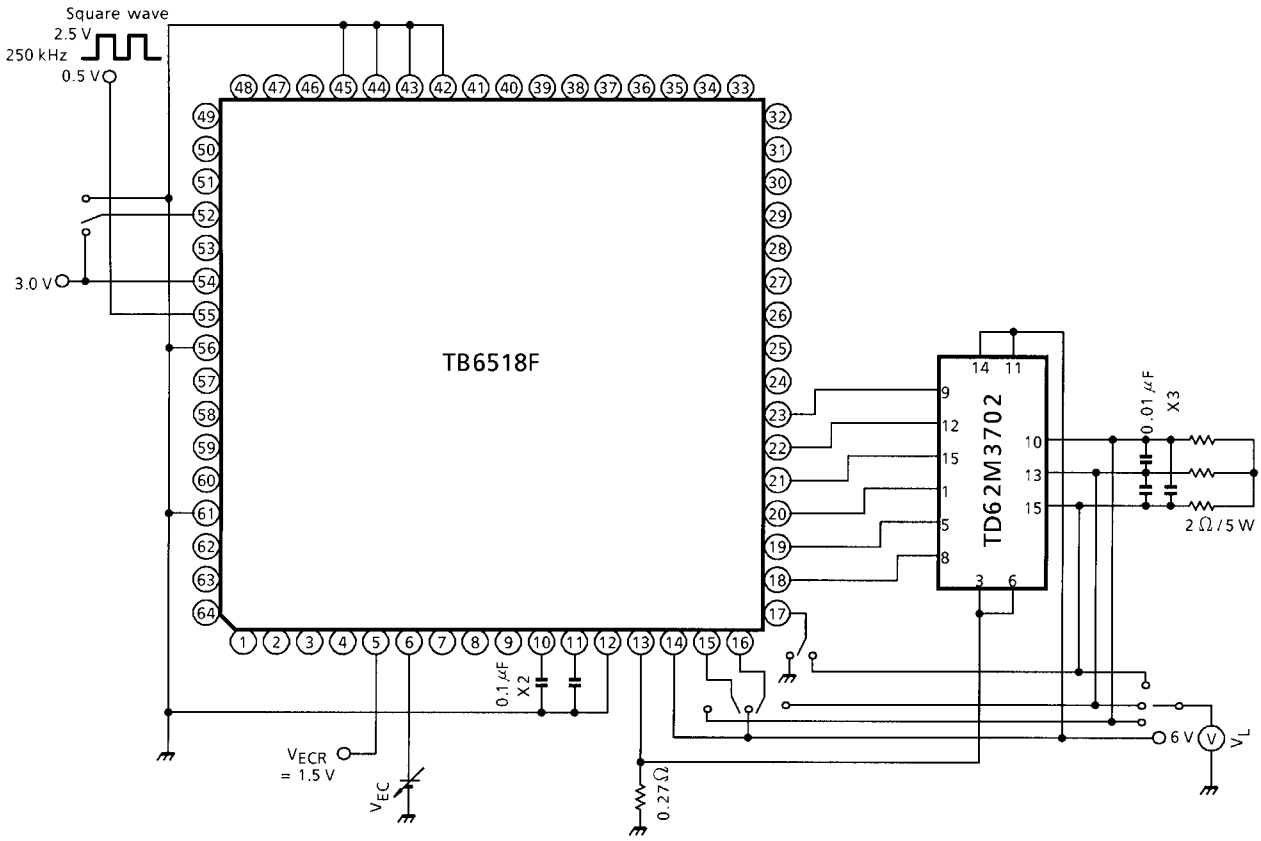
$$\Delta EC = VEC - VECR \ (VCS \approx 0\ V)$$

$$YGio = \frac{V_{CS1} - V_{CS2}}{0.1\ V}$$

No. 22 V_{REF}

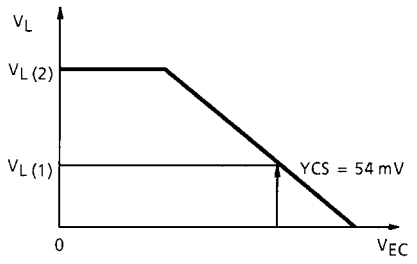
Apply 3.0 V to the V_{CC} and then measure the voltage of the REFO terminal.

TEST CIRCUIT 3. $V_{L\,(1)}$, $V_{L\,(2)}$



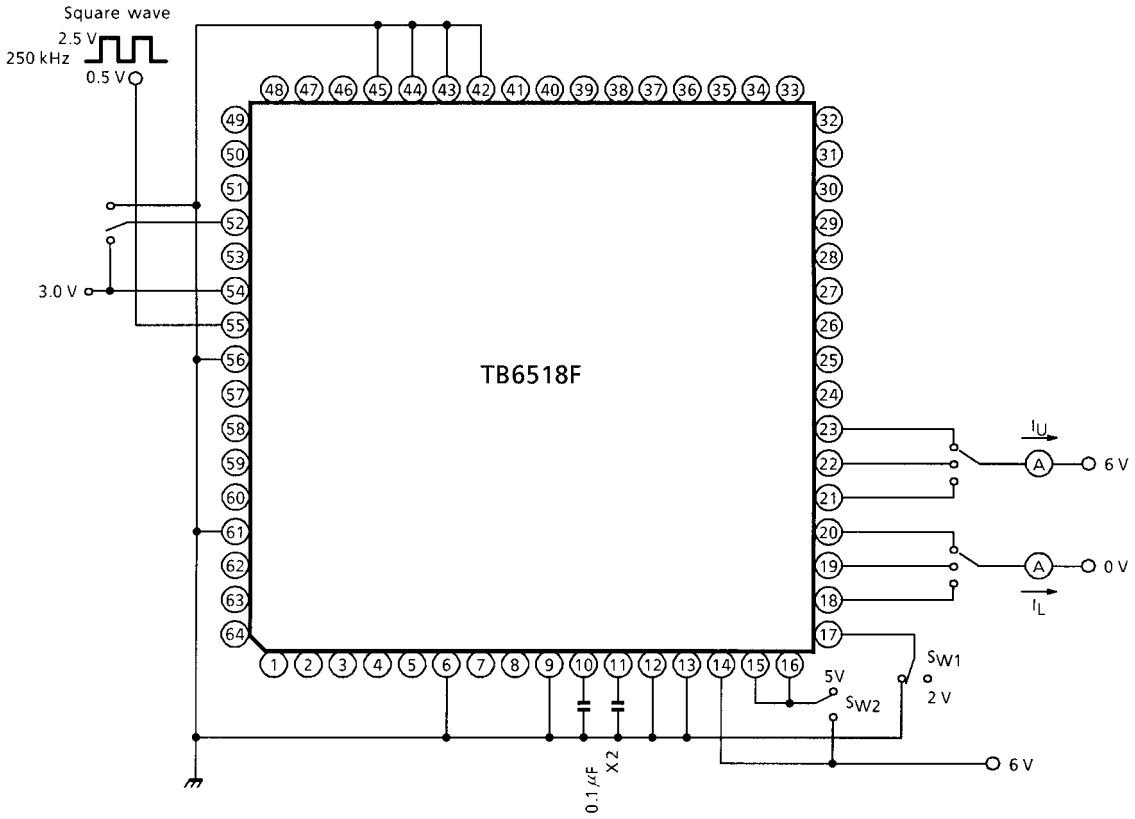
No. 8 $V_{L\,(1)}$, No. 9 $V_{L\,(2)}$

Change the YSTB terminal from H to L with YMI = 0 V, YM2 = 6 V and YM3 = 6 V and then enter the following clock counts into the YCLK terminal in order to set the drive angle.
Connect the YM1, YM2 and YM3 terminals to PWTR after setting the drive angle and then carry out the measurement.



CLOCK	80	150	270
Terminal	YM3	YM1	YM2

TEST CIRCUIT 4. I_U, I_L

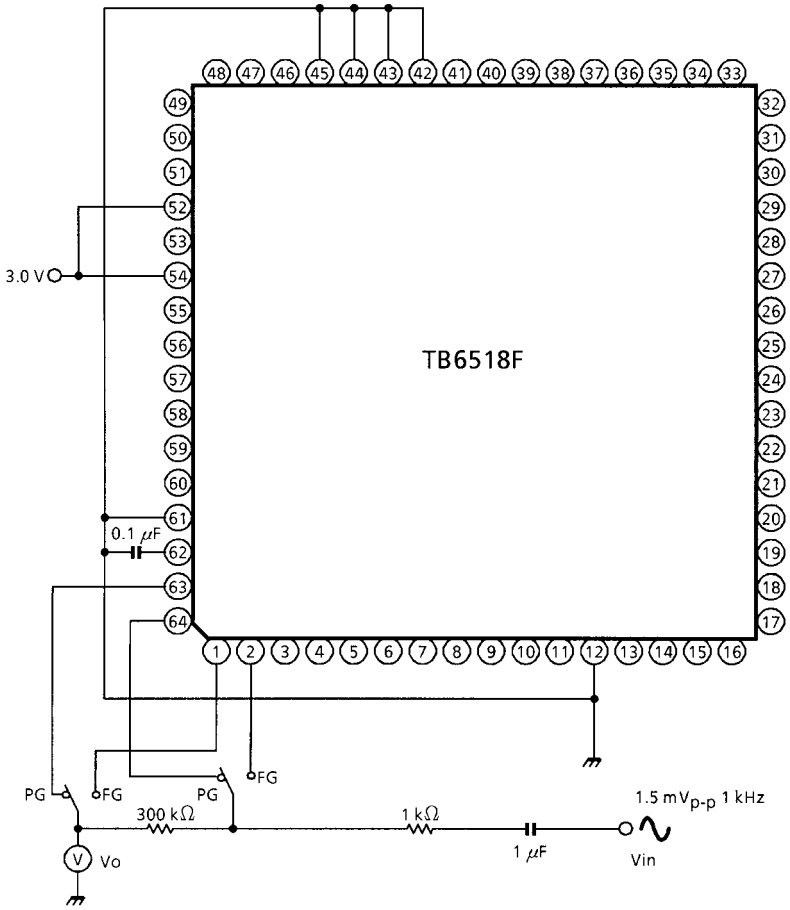


No. 10 I_U, No. 11 I_L

Change the YSTB terminal from H to L and then enter the following clock counts into the YCLK terminal in order to set the drive angle.

CLOCK	50		105		200	
Terminal	YU1	YL3	YU2	YL1	YU3	YL2
S_{W1}	0 V	2 V	0 V	2 V	0 V	2 V
S_{W2}	5 V	6 V	5 V	6 V	5 V	6 V

TEST CIRCUIT 5. G_{FG}, G_{PG}



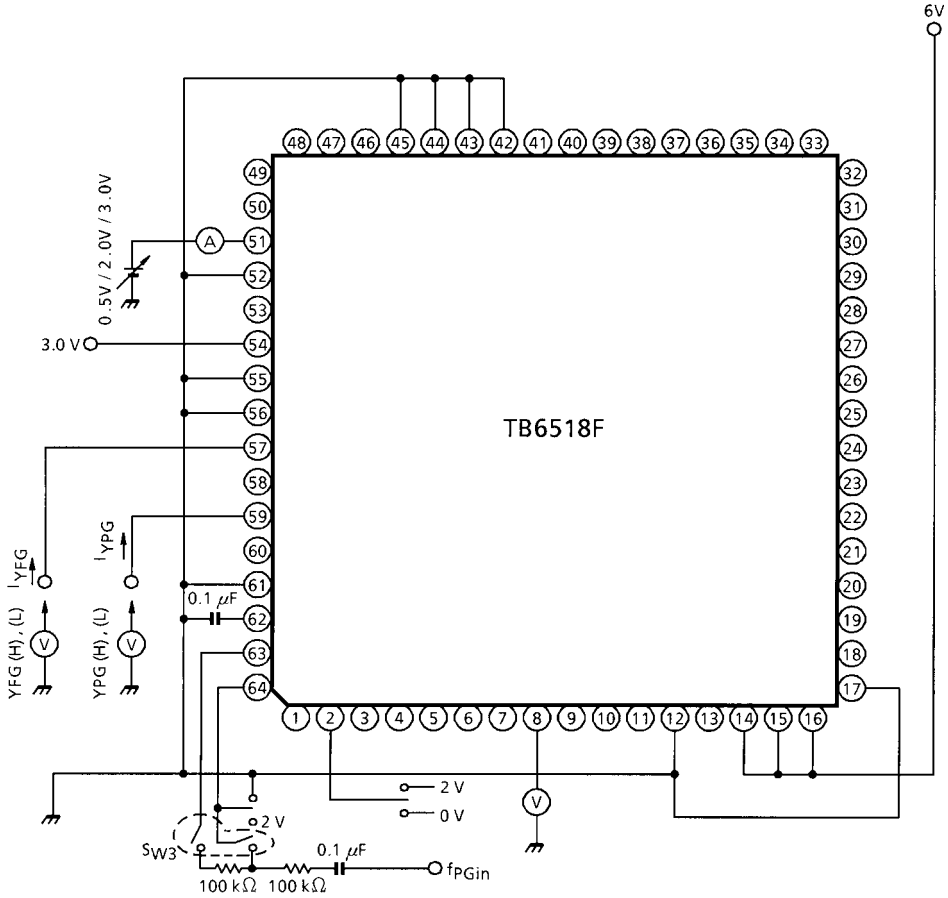
No. 12 G_{FG}

Set the SW to FG, measure Vo when Vin = 1.5 mV_{p-p} at 1 kHz and acquire $G_{FG} = 20 \log (Vo / Vin)$.

No. 15 G_{PG}

Set the SW to PG, measure Vo when Vin = 1.5 mV_{p-p} at 1 kHz and acquire $G_{PG} = 20 \log (Vo / Vin)$.

TEST CIRCUIT 6. YFG (H), YFG (L), ΔPGin, YPG (H), YPG (L), V_{NTSC}, V_{PAL}, $I_{N/P}$



No. 13 YFG (H)

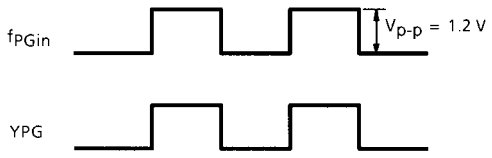
Measure the potential of YFG when a current of I_{YFG} = −100 μA is flowing after 2 V has been applied to YFGin and YFG has been set at H.

No. 14 YFG (L)

Measure the potential of YFG when a current of I_{YFG} = −100 μA is flowing after 0 V has been applied to YFGin and YFG has been set at L.

No. 16 ΔPGin

Set SW3 on, input a 10 kHz square wave from f_{PGin}, set the f_{PGin} V_{p-p} to 1.2 V (ΔPGin = 0.6 V) and confirm that the YPG terminal is operating.
Also, set V_{p-p} to 0.8 V (ΔPGin = 0.4 V) and confirm that the YPG terminal is not operating.



No. 17 YPG (H)

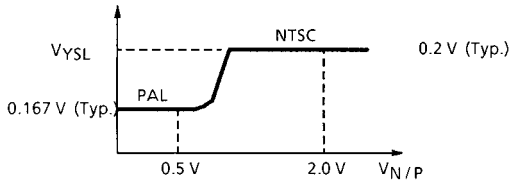
Measure the potential of YPG when a current of I_{YPG} = −100 μA is flowing after 2 V has been applied to YPGin and YPG has been set at H.

No. 18 YPG (L)

Measure the potential of YPG when a current of I_{YPG} = 100 μA is flowing after 0 V has been applied to YPGin and YPG has been set at L.

No. 25 V_{NTSC}, No.26 V_{PAL}

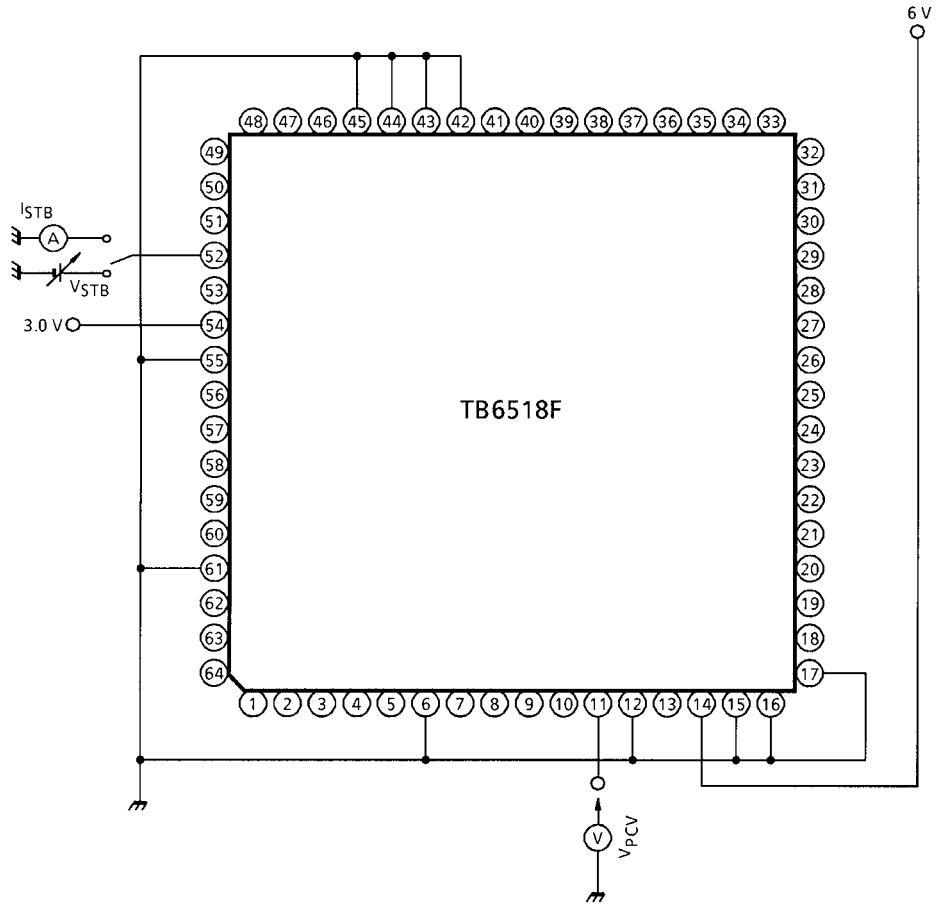
Confirm that 1.21 V is being applied to the YSUL terminal and that the voltage of the YSL terminal changes when the voltage applied to the N / P terminal is changed from 0.5 V to 2.0 V.



No. 27 $I_{N / P}$

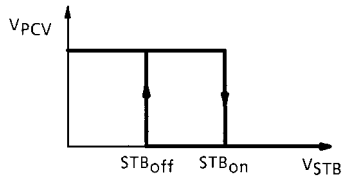
Apply 3.0 V to the N / P terminal and measure the current flowing into the terminal.

TEST CIRCUIT 7. STB_{on}, STB_{off}, I_{STB}



No. 19 STB_{on}, No. 20 STB_{off}

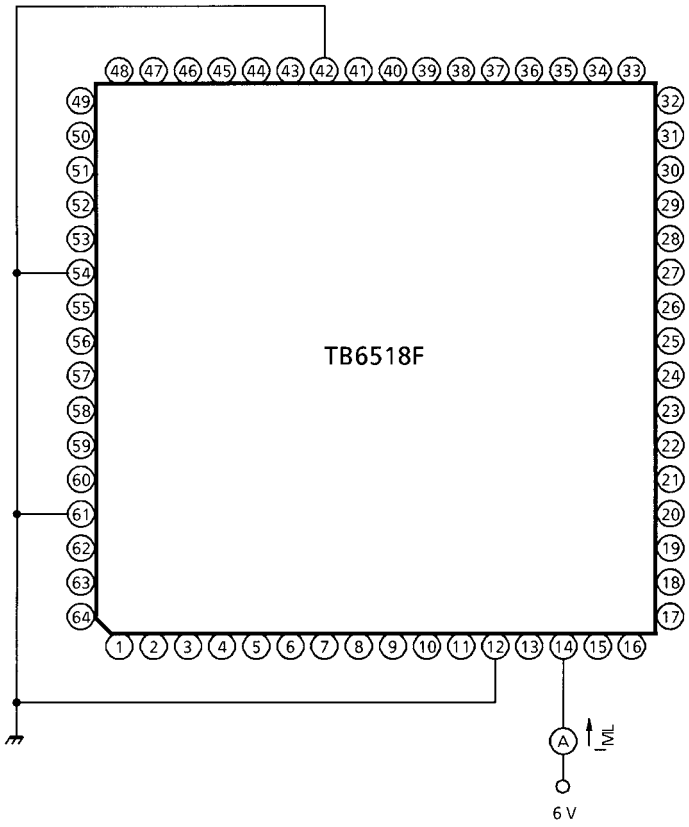
Change V_{STB} from 0 V to 3 V, and then from 3 V to 0 V, and measure V_{PCV}.
V_{STB} becomes STB_{on} when V_{PCV} changes from H to L, and becomes STB_{off} when V_{PCV} changes from L to H.



No. 21 I_{STB}

Measure I_{STB} when $V_{STB} = 0$ V

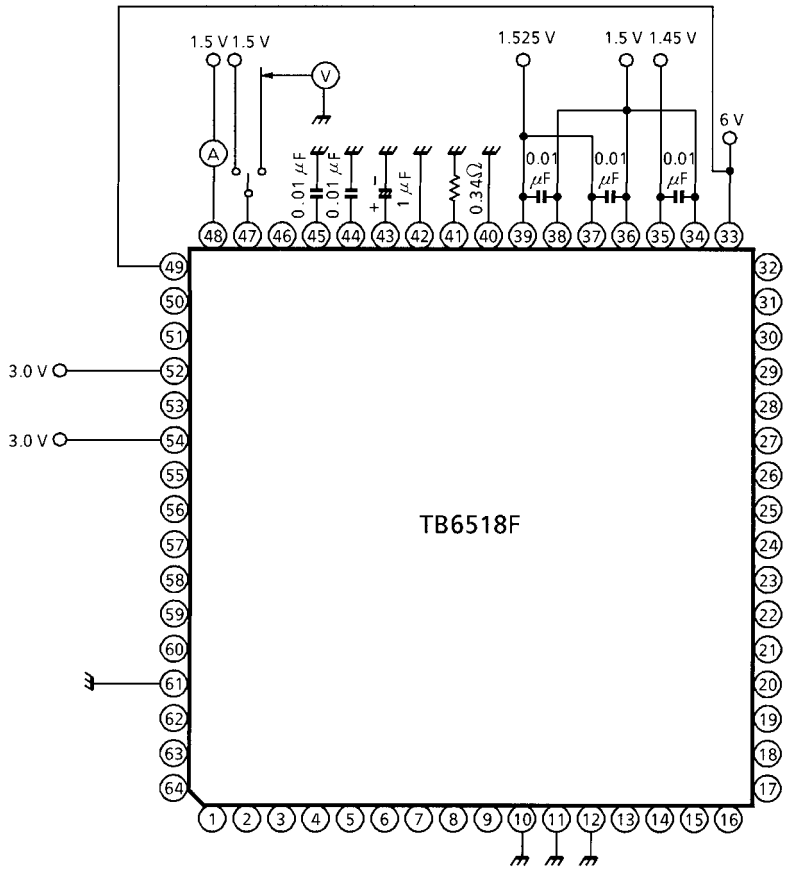
TEST CIRCUIT 8. I_{ML}



No. 23 I_{ML}

Measure the current that flows into pin (14) when YVM = 6 V.

TEST CIRCUIT 9. CI_{EC}, CE_{CR}



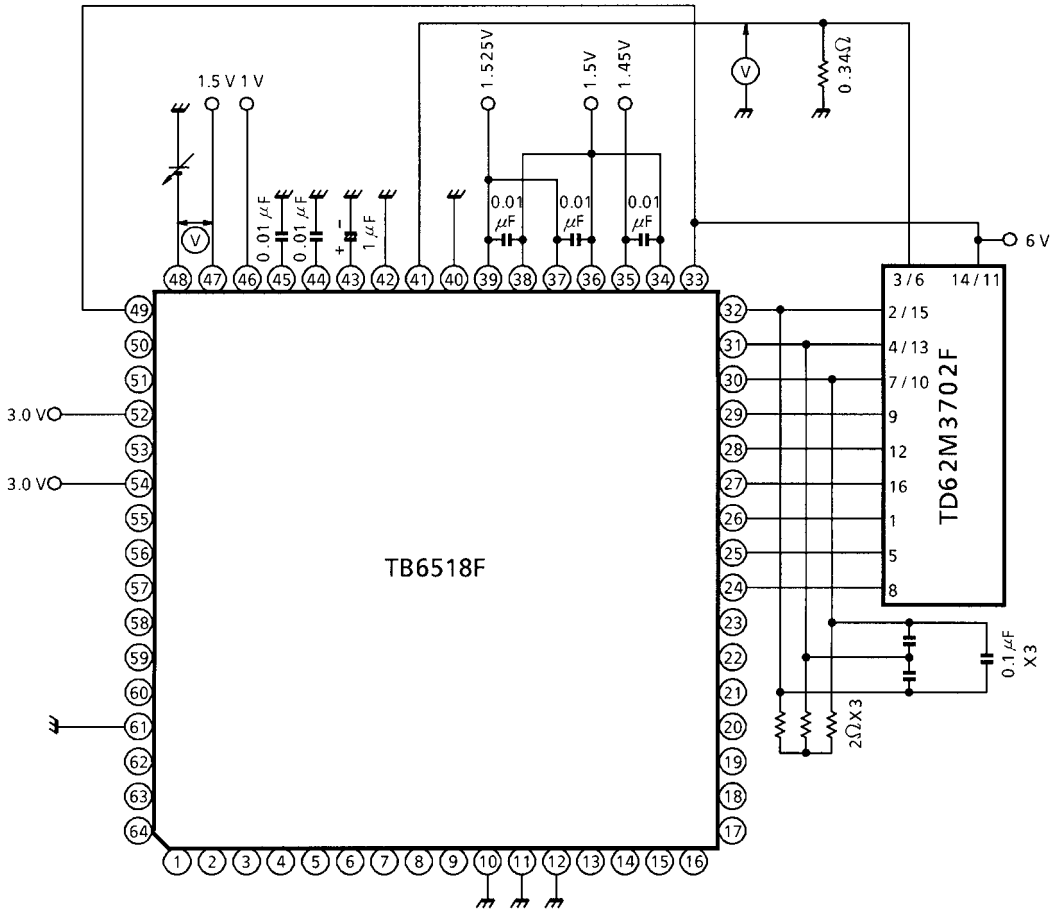
No. 28 CI_{EC}

Measure the current that flows into the CEC terminal with CEC = 1.5 V and CECR = 1.5 V.

No. 29 CE_{CR}

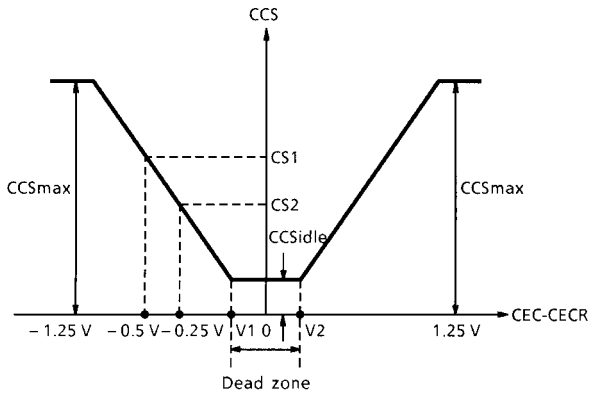
Measure the voltage of the CECR terminal.

TEST CIRCUIT 10. CEC, CCSmax, CGio, CCSidle, CECofs, CECdz



No. 30 No. 31 No. 32 No. 33 No. 34 No. 35

Set CTL = 1.0 V and CECR = 1.5 V, change CEC from 0 V to 3.0 V, measure the potential of the CCS terminal and confirm the V characteristics.



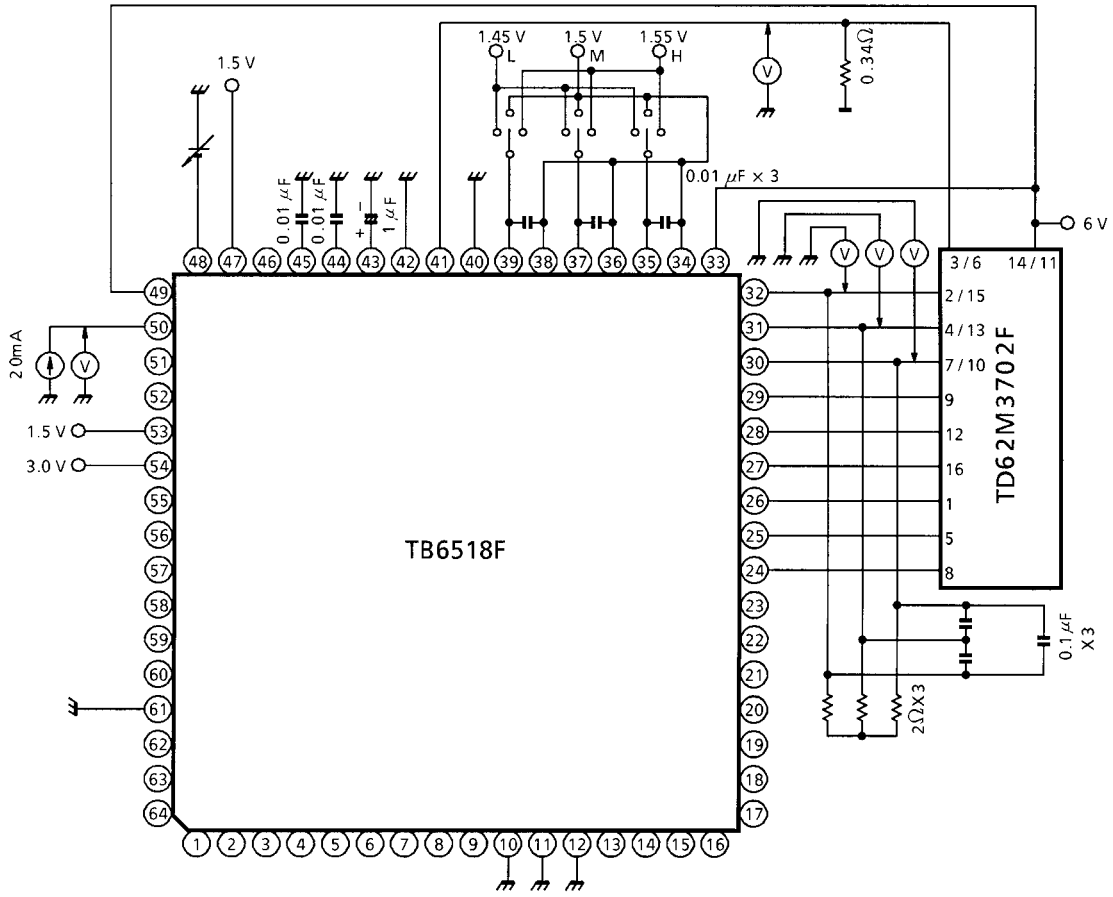
$$CGio = \frac{CS1 - CS2}{0.25\ V}$$

CCSidle : The CS potential within the dead zone

$$CECofs = \frac{V1 + V2}{2}$$

$$CECdz = V2 - V1$$

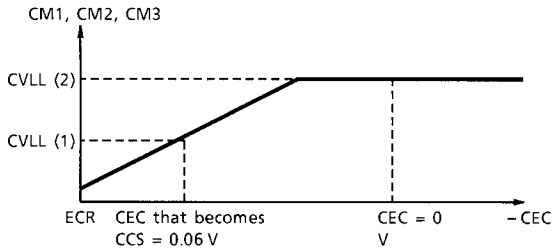
TEST CIRCUIT 11. CVLL (1), CVLL (2)



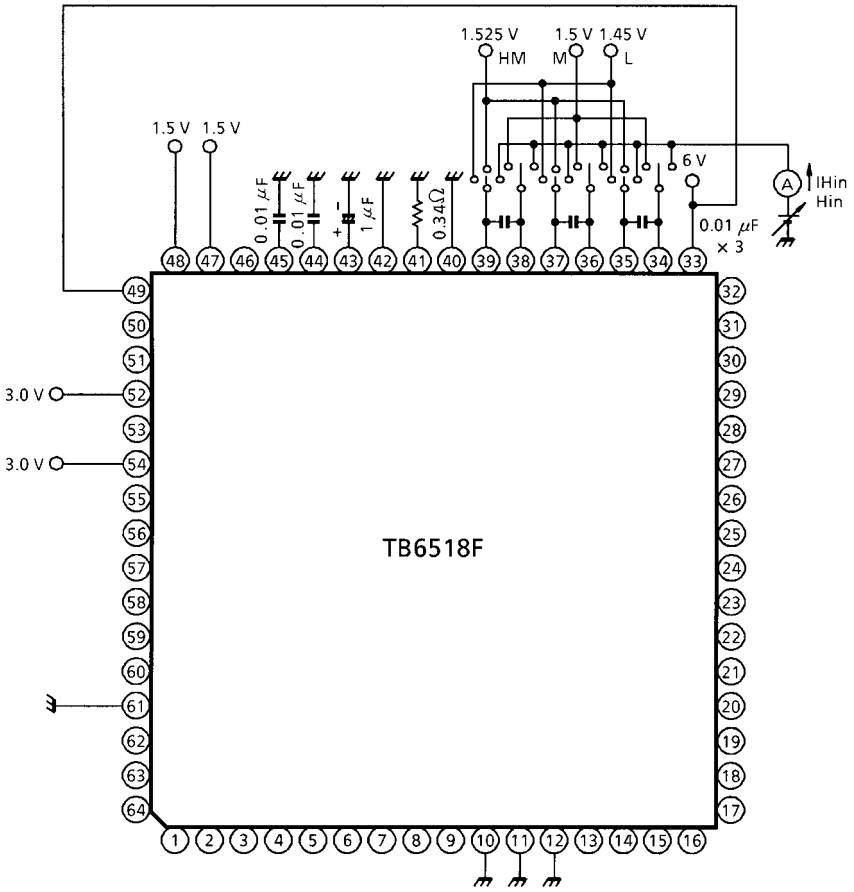
No. 36 CVLL (1), No. 37 CVLL (2)

Perform the settings laid out in the table below and measure the potential of the CM1, CM2 and CM3 terminals when the CEC voltage is adjusted to CCS = 0.06 V and when CEC = 0 V.

	H1+	H2+	H3+	TEST TERMINAL
Setting 1	H	L	M	CM1
Setting 2	M	H	L	CM2
Setting 3	L	M	H	CM3



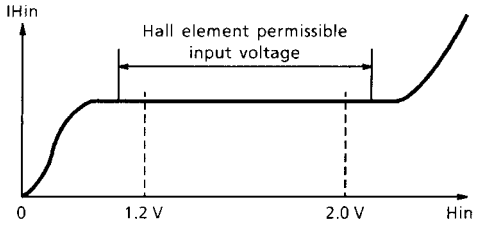
TEST CIRCUIT 12. Hin



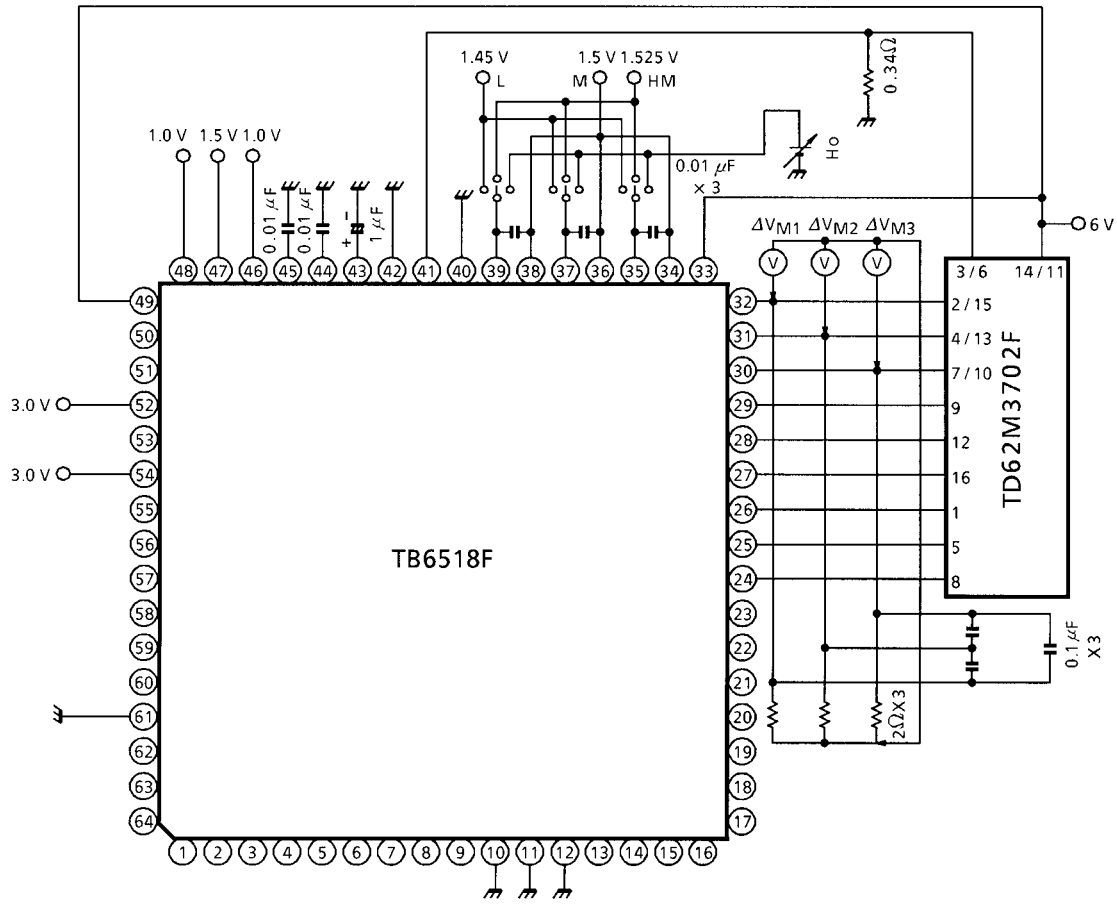
No. 38 Hin

Perform the settings laid out in the table below and then measure the voltage range of the IHin that does change rapidly in accordance with changes in the Hin.

	H1+	H1−	H2+	H2−	H3+	H3−
Setting 1	Hin	Hin	HM	M	L	M
Setting 2	L	M	Hin	Hin	HM	M
Setting 3	HM	M	L	M	Hin	Hin



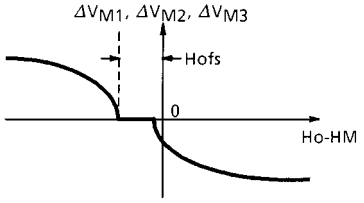
TEST CIRCUIT 13. Hofs



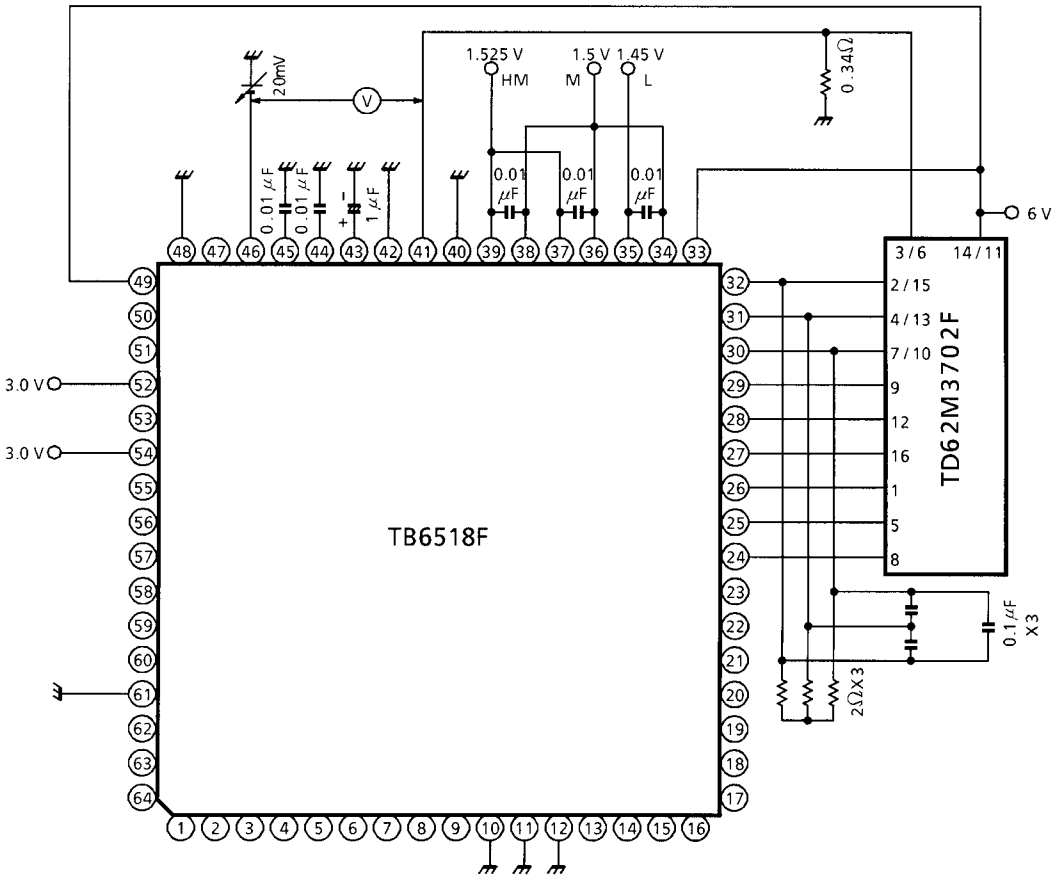
No. 39 Hofs

Perform the settings laid out in the table below and then measure the hall element input conversion offset.

	H1+	H2+	H3+	OFFSET MEASUREMENT
Setting 1	Ho	HM	L	ΔV_{M1} = 0 difference between H1+ and H2+
Setting 2	L	Ho	HM	ΔV_{M2} = 0 difference between H2+ and H3+
Setting 3	HM	L	Ho	ΔV_{M3} = 0 difference between H3+ and H1+

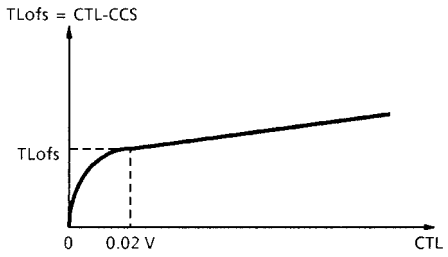


TEST CIRCUIT 14. TLofs

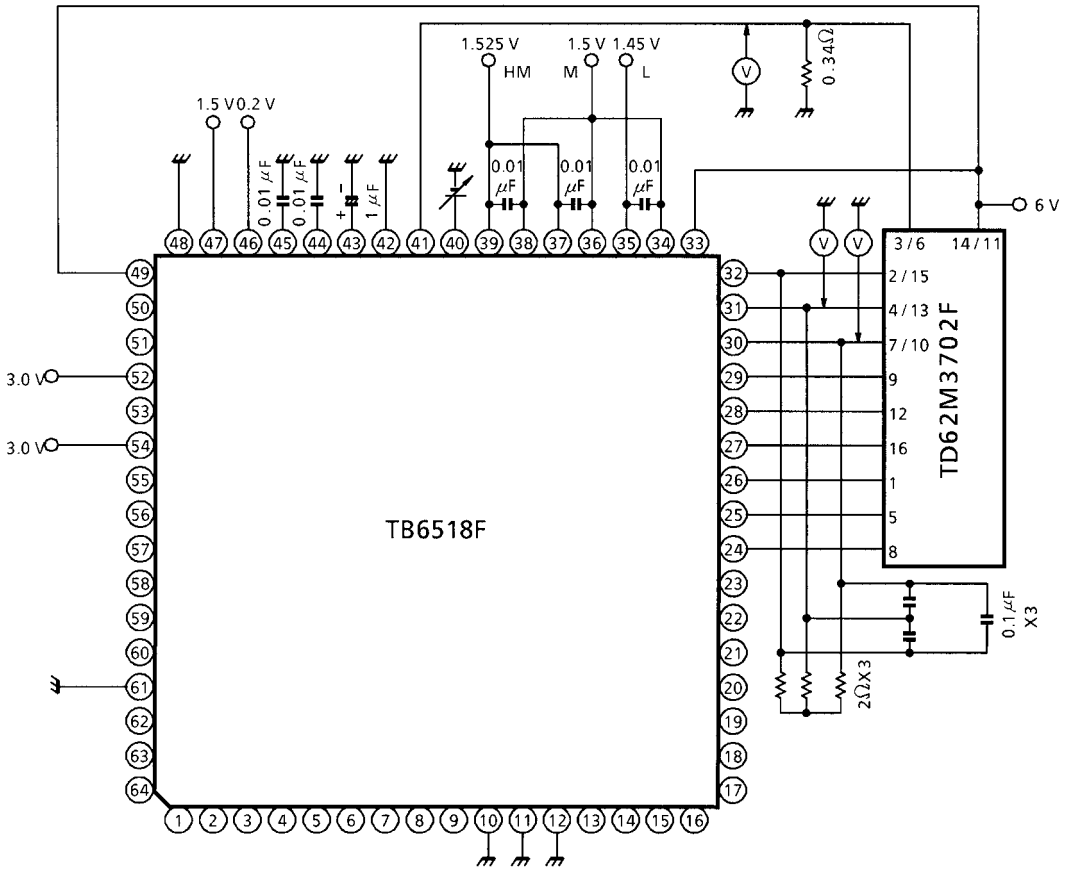


No. 40 TLofs

Measure the potential differential (CTL−CCS) of the CTL and CCS terminals when CTL = 0.02 V.

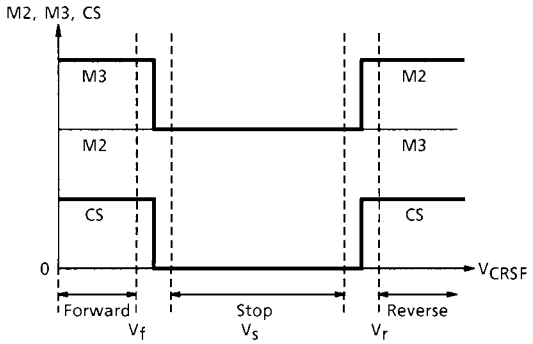


TEST CIRCUIT 15. V_f, V_s, V_r

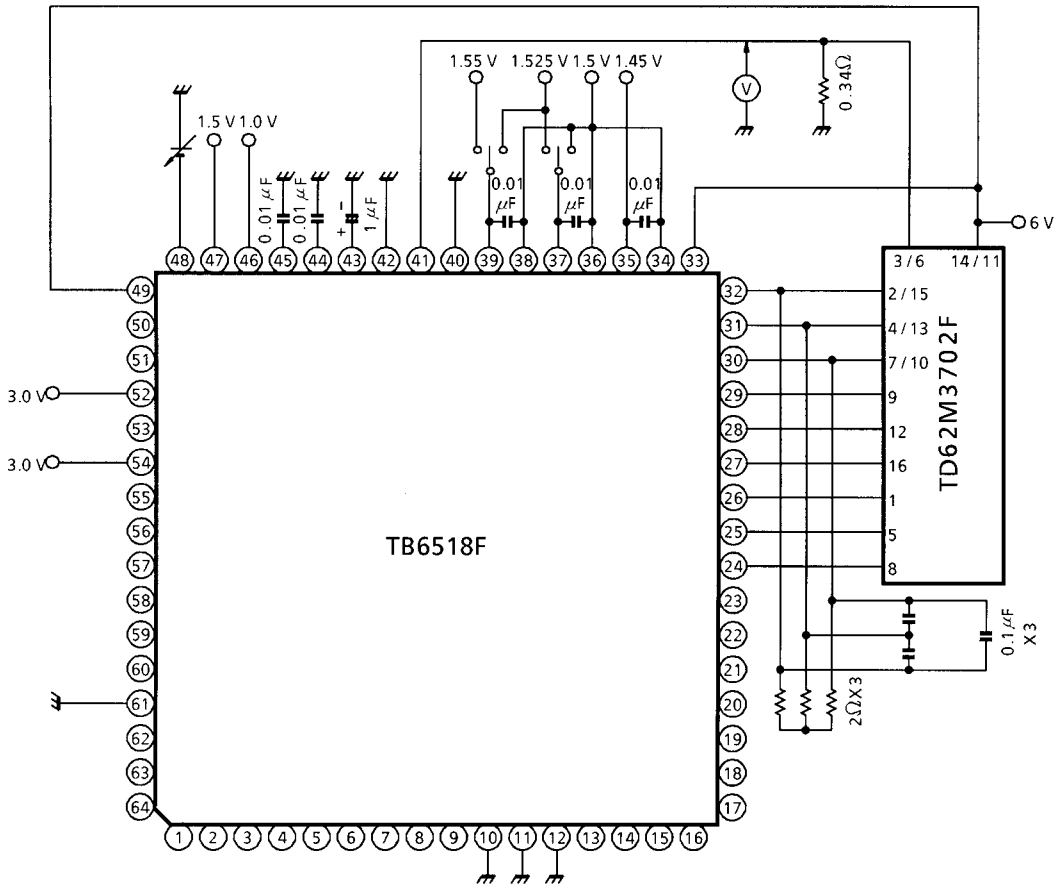


No. 41 Vf, No. 42 Vs, No. 43 Vr

Change CRSF from 0 V to 3.5 V, acquire the characteristics indicated in the following diagram and measure the threshold voltage.



TEST CIRCUIT 16. R

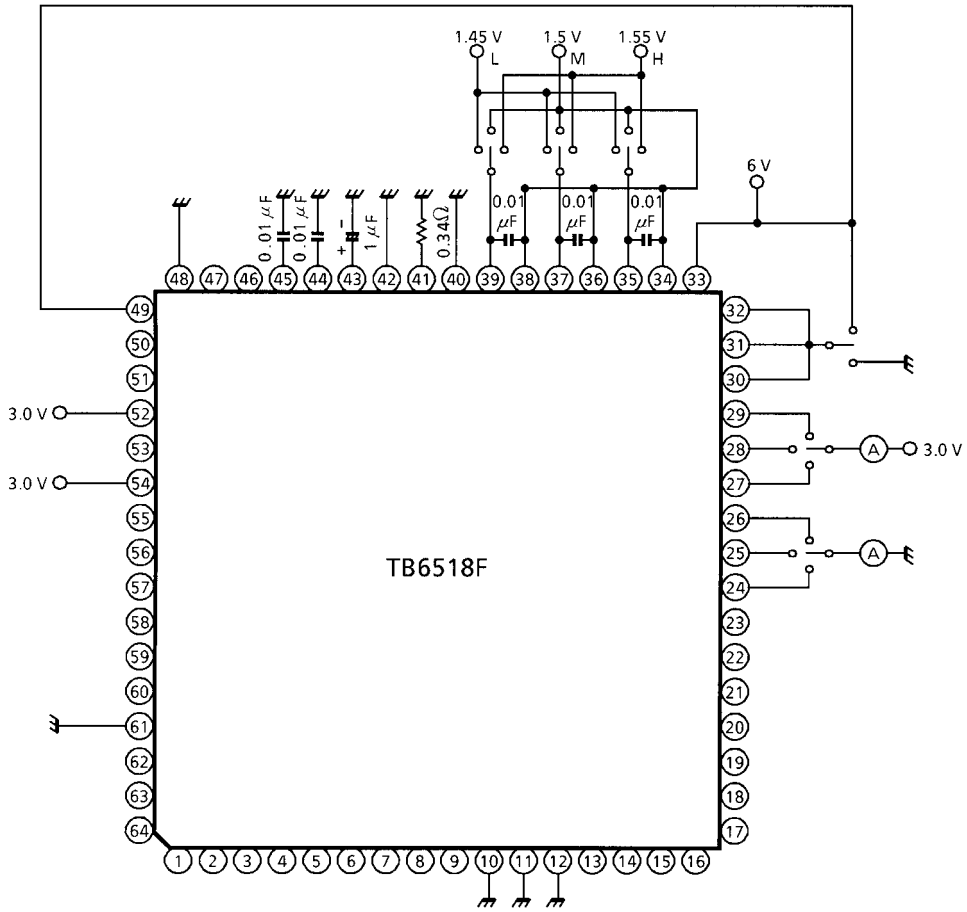


No. 44 R

Adjust the CEC voltage so that CCS becomes 0.06 V with H1+ = 1.525 V and H2+ = 1.525 V, and then measure CCS (CS_L) when H1+ = 1.525 V and H2+ = 1.525 V and CCS (CS_H) when H1+ = 1.55 V and H2+ = 1.5 V.

Then acquire : $R = \dfrac{CS_H - CS_L}{CS_L}$

TEST CIRCUIT 17. CI_U, CI_L

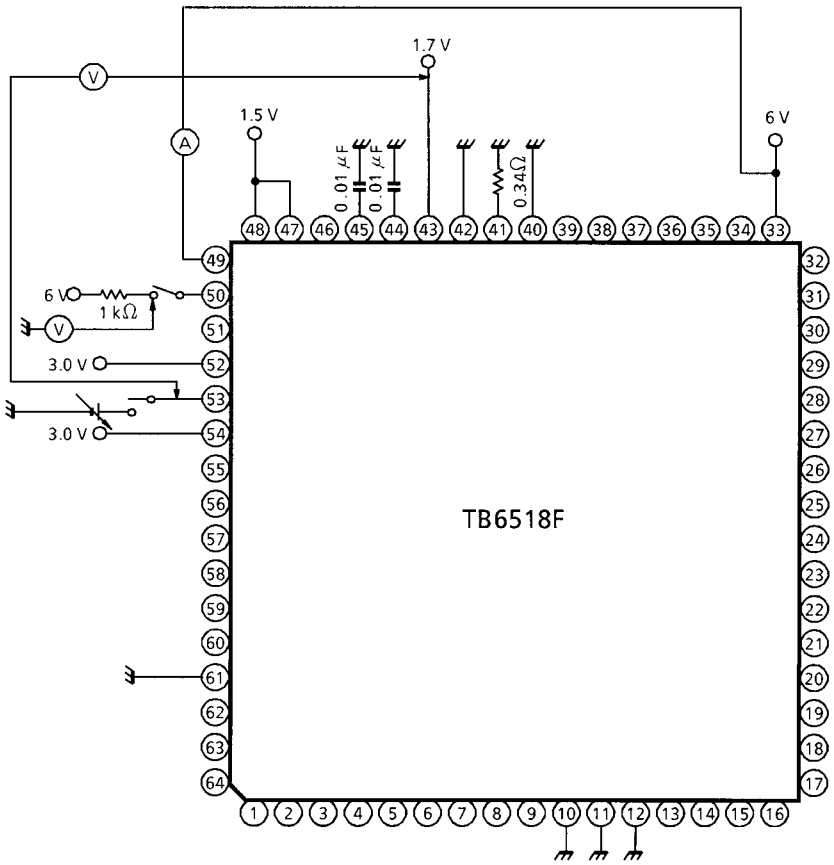


No. 45 CI_U, No. 46 CI_L

Perform the settings laid out in the table below and then measure the current that flows into the CU1, CU2 and CU3 terminals, and the CL1, CL2 and CL3 terminals.

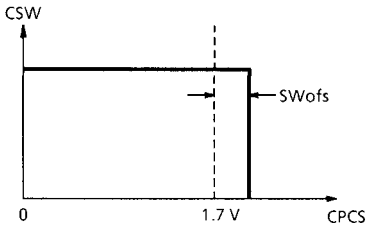
	H1+	H2+	H3+	M1, M2, M3	TEST TERMINAL
Setting 1	L	H	M	GND	CU1
Setting 2	M	L	H	GND	CU2
Setting 3	H	M	L	GND	CU3
Setting 4	H	L	M	V_M	CL1
Setting 5	M	H	L	V_M	CL2
Setting 6	L	M	H	V_M	CL3

TEST CIRCUIT 18. CSWofs, I_{REG}



No. 47 CSWofs

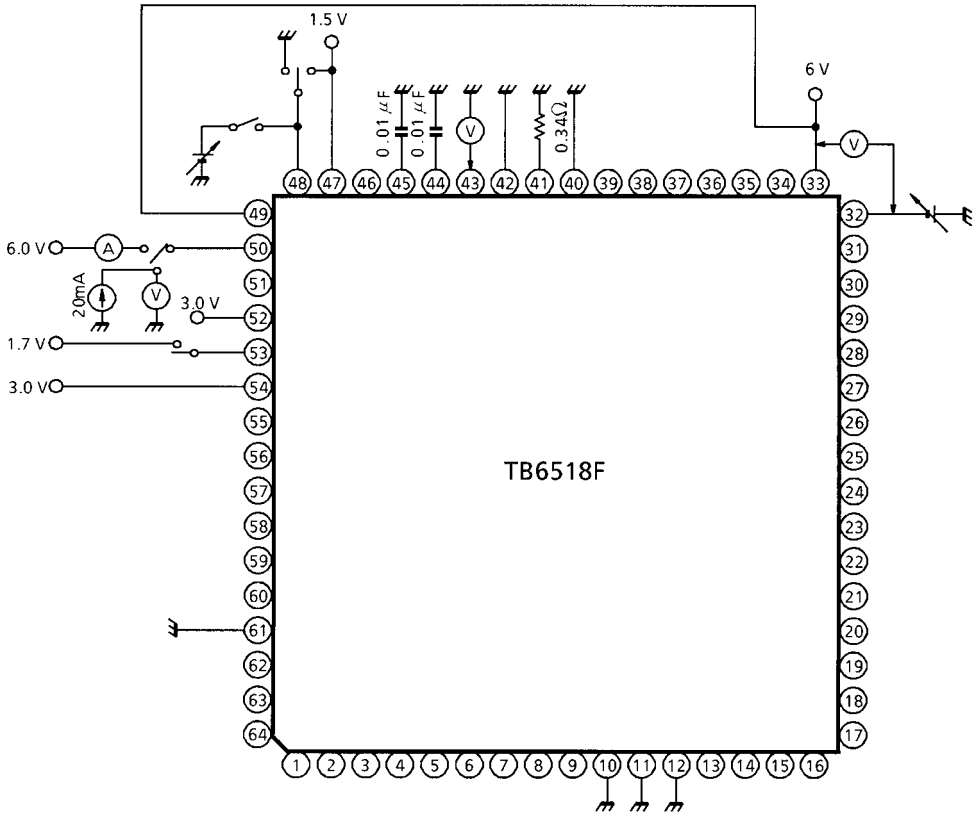
Set SPCS = 1.7 V, change FC from 0 V to 3.0 V and measure the potential difference (FC − CPCS) of the FC terminal and the CPCS terminal when CSW changes from high to low.



No. 58 I_{REG}

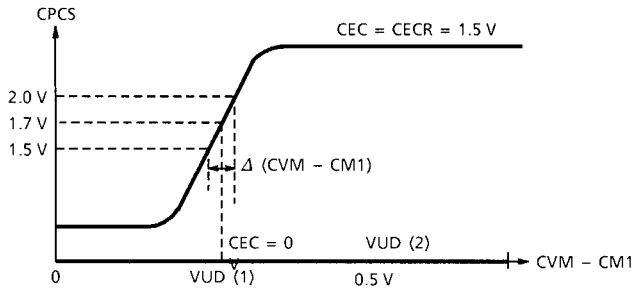
Measure the current of the NOREG terminal when 6 V is applied with CVM = 6 V and FC = 1.8 V, and with the CSW terminal open.

TEST CIRCUIT 19. CG_{PCS}, VUD (1), VUD (2), CI_{SWB}, SWEC



No. 48 CG_{PCS}, No. 49 VUD (1), No. 50 VUD (2)

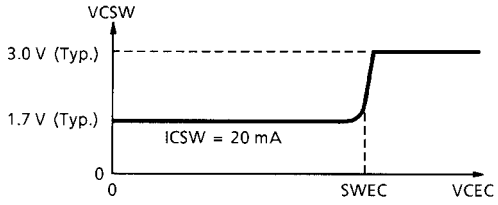
Set CEC = 0 V, change CM1 from 6 V to 5 V and measure the potential difference (CVM − CM1) of the CVM terminal and the CM1 terminal when the potential of the CPCS terminal becomes 1.7 V.
Set CEC = CECR = 1.5 V, perform the same measurements as outlined below and acquire the characteristics indicated in the diagram below.



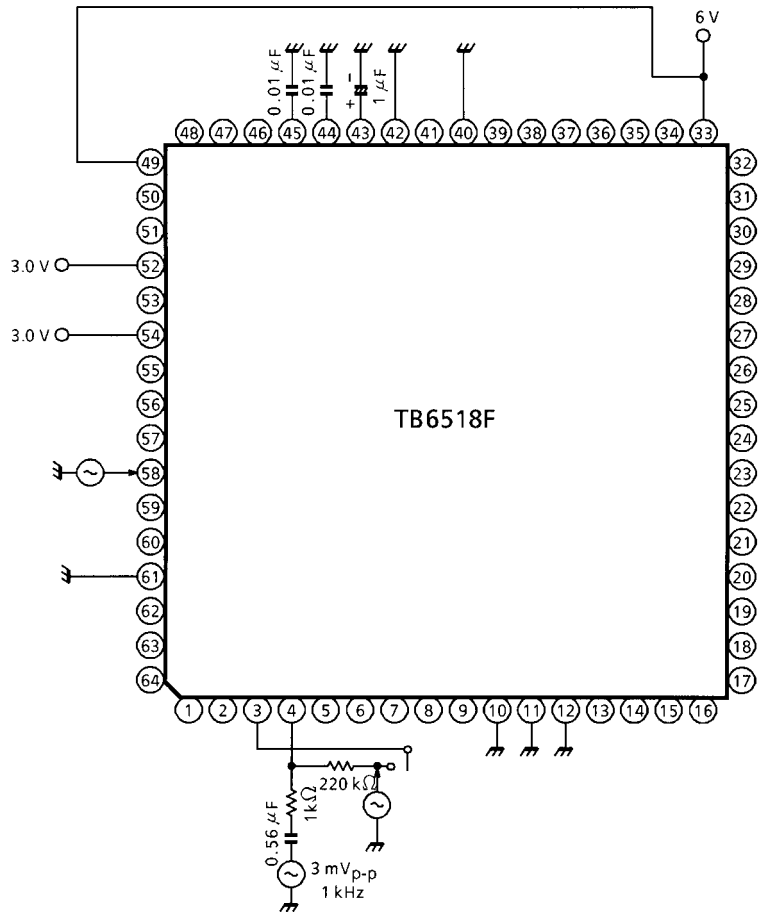
$$CG_{PCS} = \frac{2.0\,V - 1.5\,V}{\Delta(CVM - CM1)}$$

No. 51 CI_{SWB}, No. 57 SWEC

Set FC = 1.7 V, CEC = 0 V and CM1 = 6 V and measure the current that flows into the CSW terminal. Apply 10 mA to the CSW terminal, apply voltage to the CEC terminal and acquire the characteristics indicated in the diagram on the right−hand side.



TEST CIRCUIT 20. CG_{FG}, CFG_H, CFG_L

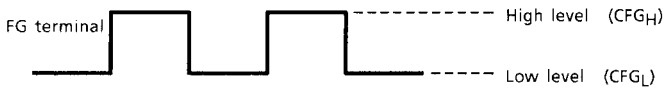


No. 52 CG_{FG} No. 53 CFG_H No. 54 CFG_L

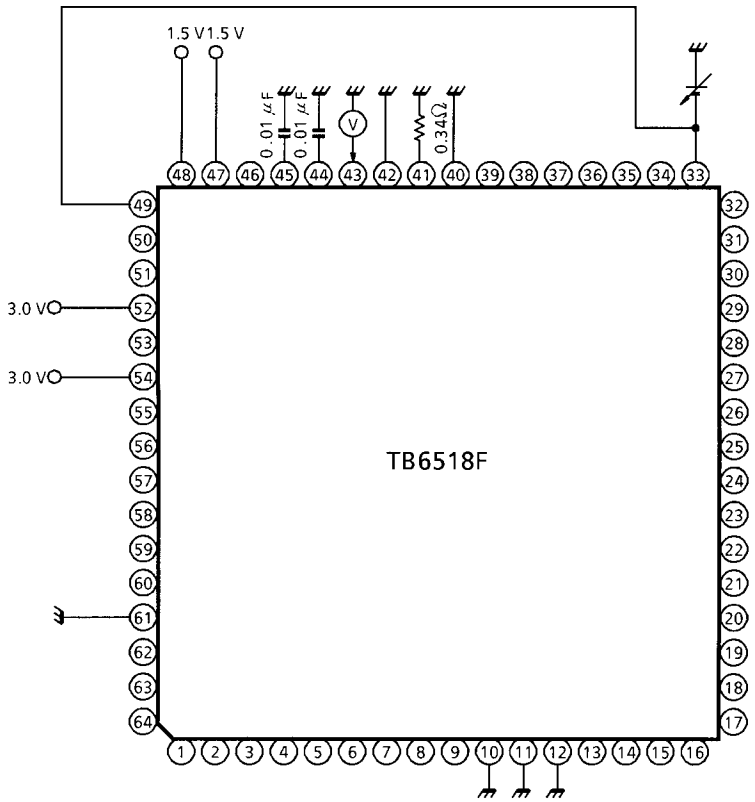
Set CFGout = Vo and measure Vo when Vin = 3 mV_{p-p} at 1 kHz.

Then acquire : $CG_{FG} = 20 \log \frac{Vo}{Vin}$

Also, acquire the characteristics indicated in the diagram below and then measure the high level potential and low level potential of the CFG terminal's output wave form.

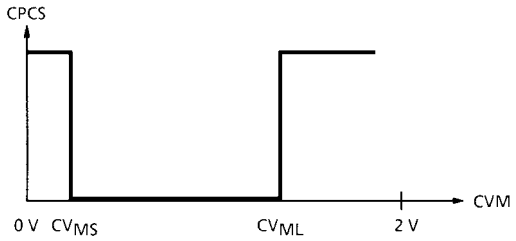


TEST CIRCUIT 21. CV_{ML}, CV_{MS}



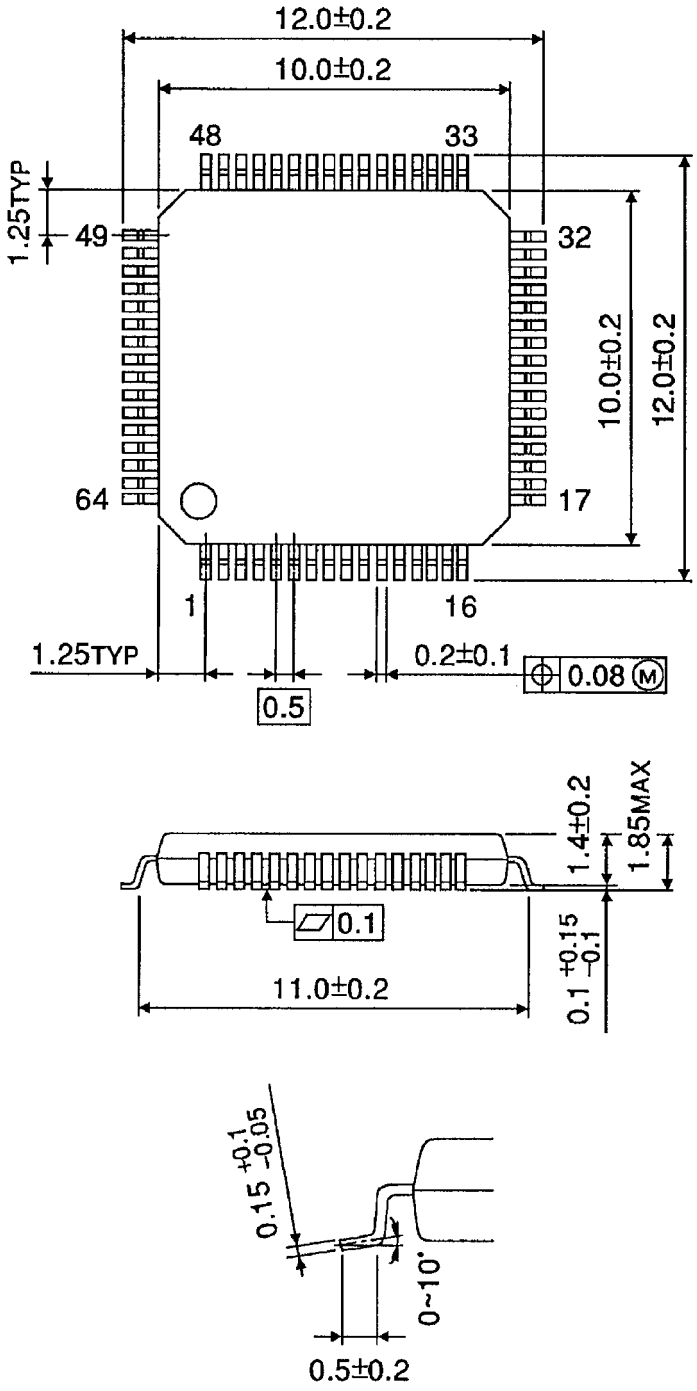
No. 55 CV_{ML} No. 56 CV_{MS}

Change CVM from 2 V to 0 V, acquire the characteristics indicated in the following diagram and measure the threshold voltage.



PACKAGE DIMENSIONS

LQFP64−P−1010−0.50A Unit: mm



Weight: 0.34 g (Typ.)

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