TC4423/TC4424/TC4425

3A Dual High-Speed Power MOSFET Drivers

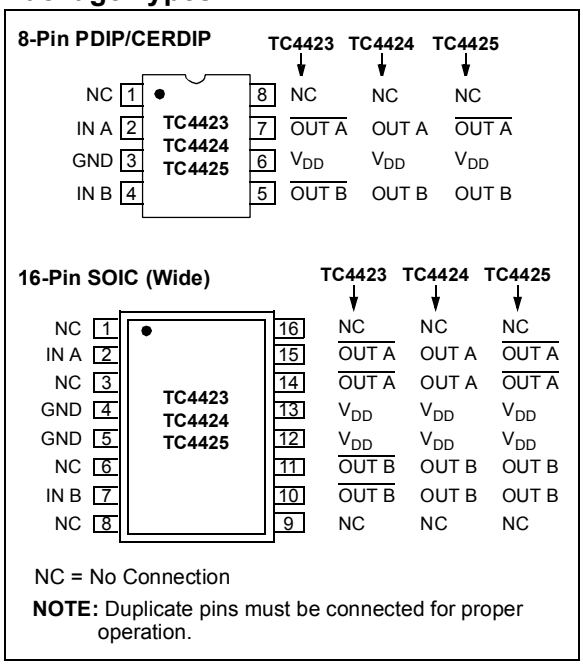
Features

- High Peak Output Current: 3A
- Wide Input Supply Operating Range:
  - 4.5V to 18V
- High Capacitive Load Drive Capability: 1800 pF in 25 nsec
- Short Delay Times: <40 nsec (Typ)
- Matched Rise/Fall Times
- Low Supply Current:
  - With Logic '1' Input – 3.5 mA
  - With Logic '0' Input – 350 µA
- Low Output Impedance: 3.5Ω (Typ)
- Latch-Up Protected: Will Withstand 1.5A Reverse Current
- Logic Input Will Withstand Negative Swing Up To 5V
- ESD Protected: 4 kV
- Pin compatible with the TC1426/TC1427/TC1428, TC4426/TC4427/TC4428 and TC4426A/ TC4427A/TC4428A devices.

Applications

- Switch Mode Power Supplies
- Pulse Transformer Drive
- Line Drivers

Package Types



NC = No Connection

NOTE: Duplicate pins must be connected for proper operation.

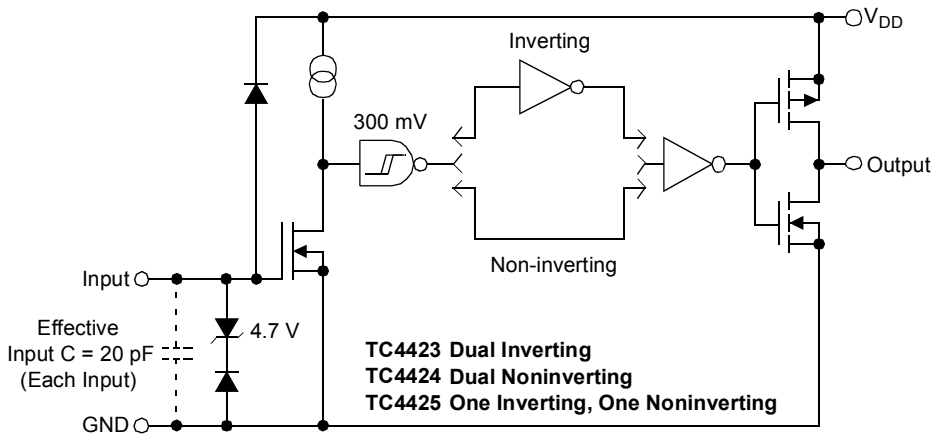
General Description

The TC4423/TC4424/TC4425 devices are a family of 3A, dual output buffers/MOSFET drivers. Pin compatible with both the TC4426/4427/4428 and TC426/427/428 families (dual 1.5A drivers), the TC4423/TC4424/TC4425 family has an increased latch-up current rating of 1.5A, making them even more robust for operation in harsh electrical environments.

As MOSFET drivers, the TC4423/TC4424/TC4425 can easily charge 1800 pF gate capacitance in under 35 nsec and provide low enough impedances in both the ON and OFF states to ensure the MOSFET's intended state will not be affected, even by large transients.

The TC4423/TC4424/TC4425 inputs may be driven directly from either TTL or CMOS (2.4V to 18V). In addition, 300 mV of hysteresis is built-in to provide noise immunity and to allow the device to be driven from slowly rising or falling waveforms.

Functional Block Diagram



Note 1: Unused inputs should be grounded.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Supply Voltage ..... +22V
Input Voltage, IN A or IN B
..... (V_{DD} + 0.3V) to (GND – 5V)
Package Power Dissipation ($T_A \leq 70°C$)
PDIP ..... 730 mW
CERDIP ..... 800 mW
SOIC ..... 470 mW
Package Thermal Resistance
CERDIP $R_{\theta J-A}$ ..... 150°C/W
CERDIP $R_{\theta J-C}$ ..... 55°C/W
PDIP $R_{\theta J-A}$ ..... 125°C/W
PDIP $R_{\theta J-C}$ ..... 45°C/W
SOIC $R_{\theta J-A}$ ..... 155°C/W
SOIC $R_{\theta J-C}$ ..... 75°C/W
Operating Temperature Range (Ambient)
C Version ..... 0°C to +70°C
E Version ..... -40°C to +85°C
M Version ..... -55°C to +125°C
V Version ..... -40°C to +125ºC
Maximum Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C

*__Notice:__ Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, with 4.5 V $\leq V_{DD} \leq$ 18 V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input						
Logic '1', High Input Voltage	V_{IH}	2.4	—	—	V	
Logic '0', Low Input Voltage	V_{IL}	—	—	0.8	V	
Input Current	I_{IN}	-1	—	1	µA	$0V \leq V_{IN} \leq V_{DD}$
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	
Low Output Voltage	V_{OL}	—	—	0.025	V	
Output Resistance, High	R_{OH}	—	2.8	5	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Output Resistance, Low	R_{OL}	—	3.5	5	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Peak Output Current	I_{PK}	—	3	—	A	
Latch-Up Protection Withstand Reverse Current	I_{REV}	—	1.5	—	A	Duty cycle ≤ 2%, t ≤ 300 µsec.
Switching Time (Note 1)						
Rise Time	t_R	—	23	35	nsec	**Figure 4-1**, **Figure 4-2**, C_L = 1800 pF
Fall Time	t_F	—	25	35	nsec	**Figure 4-1**, **Figure 4-2**, C_L = 1800 pF
Delay Time	t_{D1}	—	33	75	nsec	**Figure 4-1**, **Figure 4-2**, C_L = 1800 pF
Delay Time	t_{D2}	—	38	75	nsec	**Figure 4-1**, **Figure 4-2**, C_L = 1800 pF
Power Supply						
Power Supply Current	I_S	— —	1.5 0.15	2.5 0.25	mA	V_{IN} = 3V (Both inputs) V_{IN} = 0V (Both inputs)

Note 1: Switching times ensured by design.

ELECTRICAL CHARACTERISTICS (OPERATING TEMPERATURES)

Electrical Specifications: Unless otherwise indicated, operating temperature range with 4.5 V $\leq V_{DD} \leq$ 18 V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input						
Logic '1', High Input Voltage	V_{IH}	2.4	—	—	V	
Logic '0', Low Input Voltage	V_{IL}	—	—	0.8	V	
Input Current	I_{IN}	-10	—	+10	µA	$0V \leq V_{IN} \leq V_{DD}$
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	
Low Output Voltage	V_{OL}	—	—	0.025	V	
Output Resistance, High	R_{OH}	—	3.7	8	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Output Resistance, Low	R_{OL}	—	4.3	8	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Peak Output Current	I_{PK}	—	3.0	—	A	
Latch-Up Protection Withstand Reverse Current	I_{REV}	—	1.5	—	A	Duty cycle ≤ 2%, t ≤ 300 µsec
Switching Time (Note 1)						
Rise Time	t_R	—	28	60	nsec	**Figure 4-1**, **Figure 4-2**, C_L = 1800 pF
Fall Time	t_F	—	32	60	nsec	**Figure 4-1**, **Figure 4-2**, C_L = 1800 pF
Delay Time	t_{D1}	—	32	100	nsec	**Figure 4-1**, **Figure 4-2**, C_L = 1800 pF
Delay Time	t_{D2}	—	38	100	nsec	**Figure 4-1**, **Figure 4-2**, C_L = 1800 pF
Power Supply						
Power Supply Current	I_S	— —	2.0 0.2	3.5 0.3	mA	V_{IN} = 3V (Both inputs) V_{IN} = 0V (Both inputs)

Note 1: Switching times ensured by design.

THERMAL PACKAGE RESISTANCES

Thermal Resistance, 8L-PDIP	θ_{JA}	—	125	—	°C/W	
Thermal Resistance, 8L-CERDIP	θ_{JA}	—	150	—	°C/W	
Thermal Resistance, 16L-SOIC	θ_{JA}	—	155	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

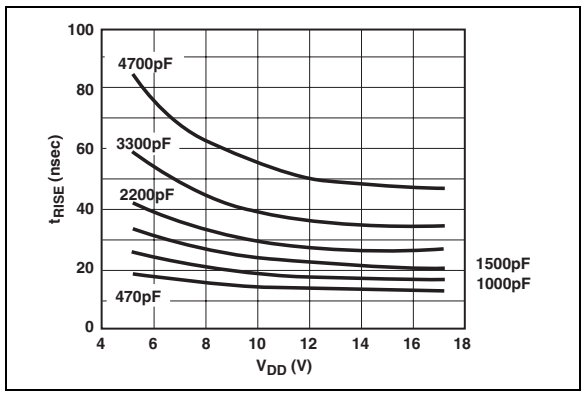


FIGURE 2-1: *Rise Time vs. Supply Voltage.*

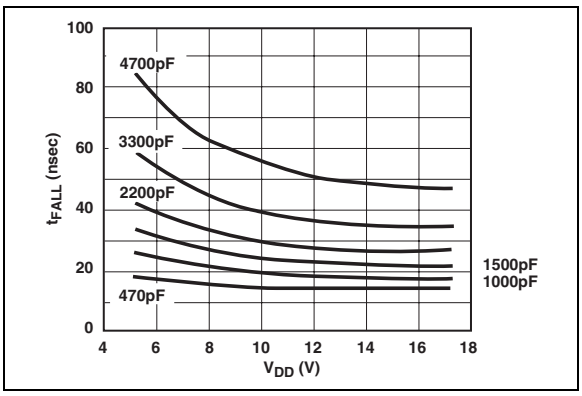


FIGURE 2-4: *Fall Time vs. Supply Voltage.*

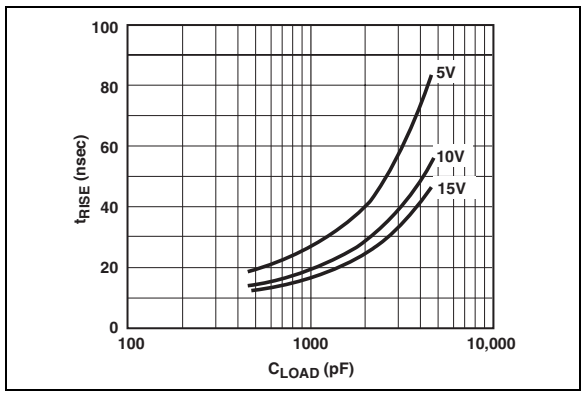


FIGURE 2-2: *Rise Time vs. Capacitive Load.*

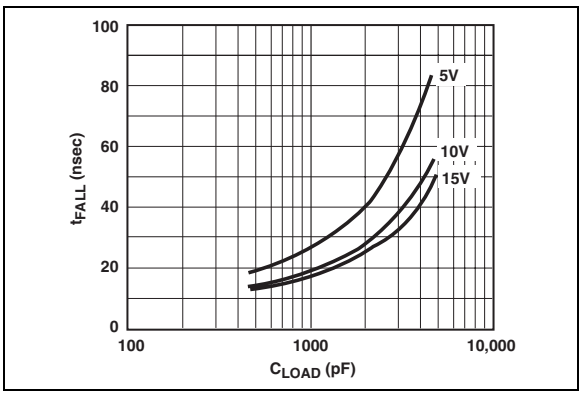


FIGURE 2-5: *Fall Time vs. Capacitive Load.*

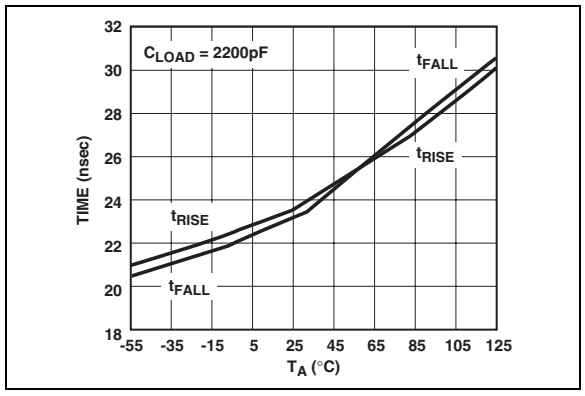


FIGURE 2-3: *Rise and Fall Times vs. Temperature.*

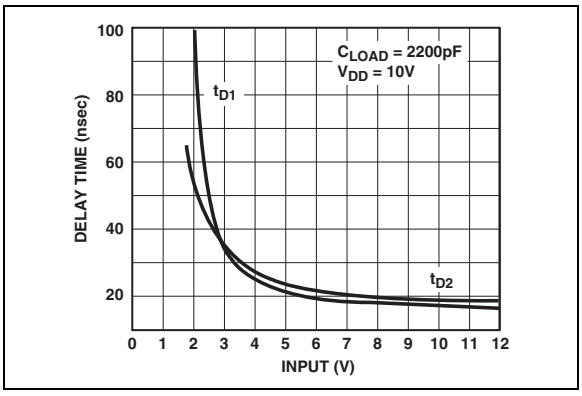


FIGURE 2-6: *Propagation Delay vs. Input Amplitude.*

Typical Performance Curves (Continued)

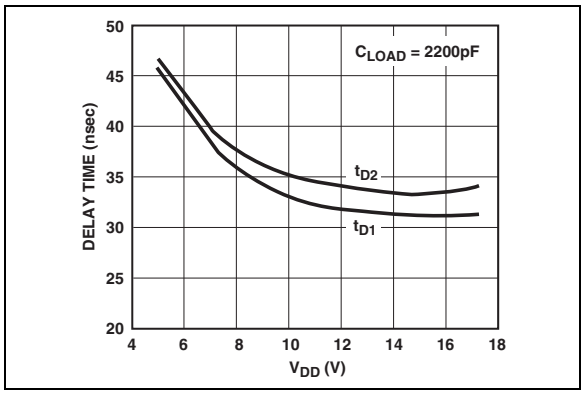


FIGURE 2-7: *Propagation Delay Time vs. Supply Voltage.*

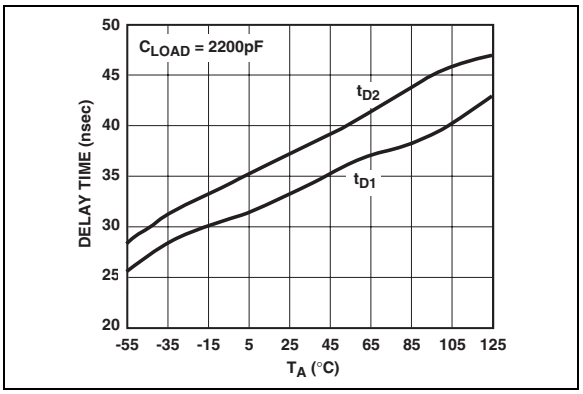


FIGURE 2-10: *Propagation Delay Time vs. Temperature.*

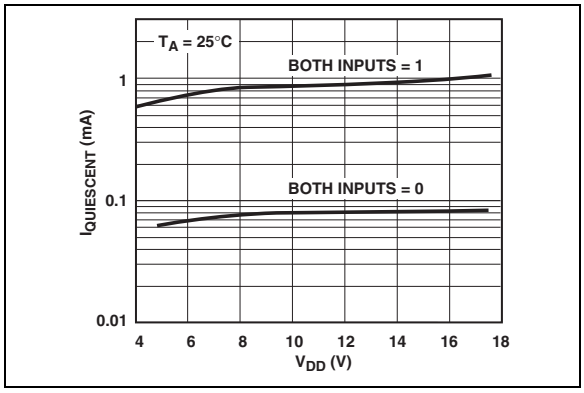


FIGURE 2-8: *Quiescent Current vs. Supply Voltage.*

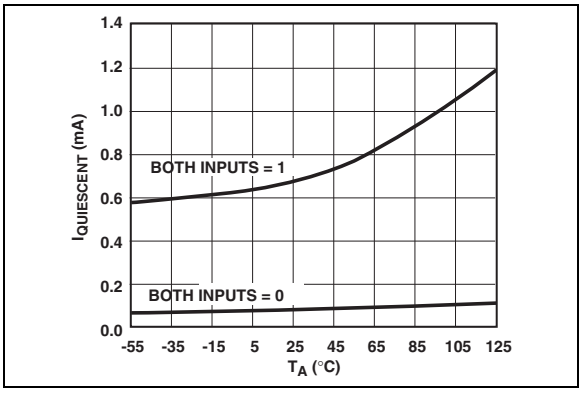


FIGURE 2-11: *Quiescent Current vs. Temperature.*

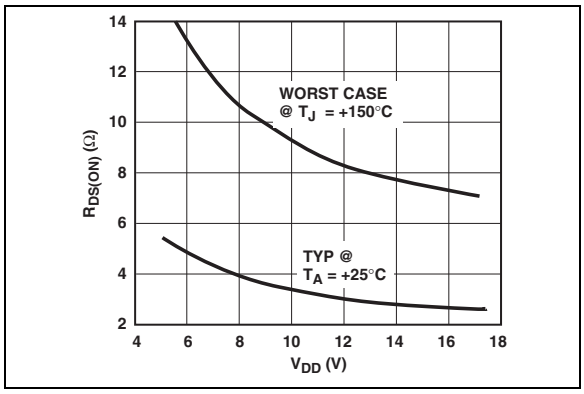


FIGURE 2-9: *Output Resistance (Output High) vs. Supply Voltage.*

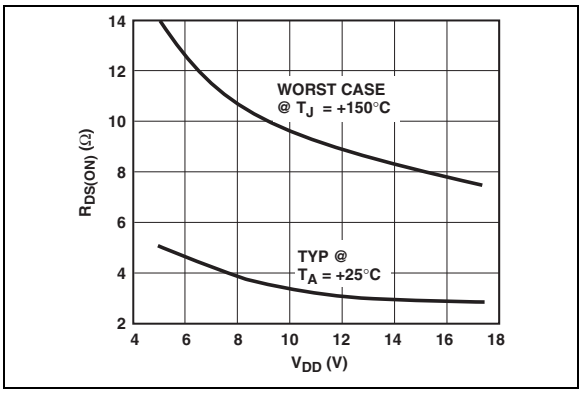


FIGURE 2-12: *Output Resistance (Output Low) vs. Supply Voltage.*

Typical Performance Curves (Continued)

Note: Load on single output only

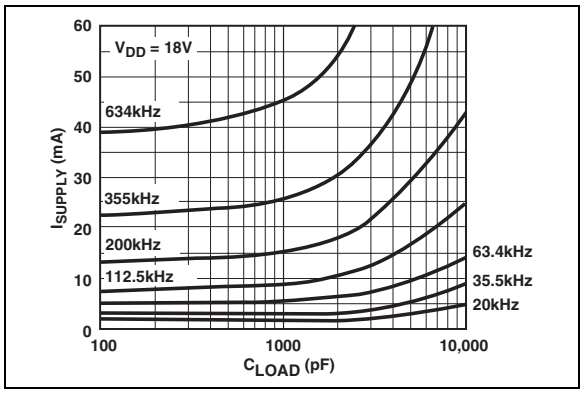


FIGURE 2-13: *Supply Current vs. Capacitive Load.*

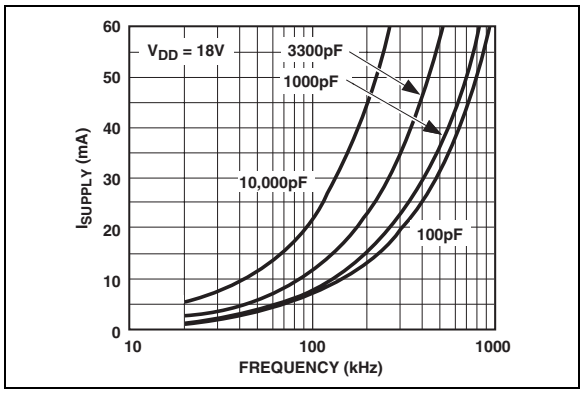


FIGURE 2-16: *Supply Current vs. Frequency.*

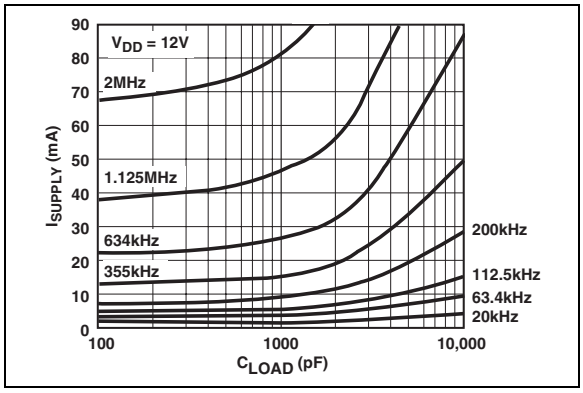


FIGURE 2-14: *Supply Current vs. Capacitive Load.*

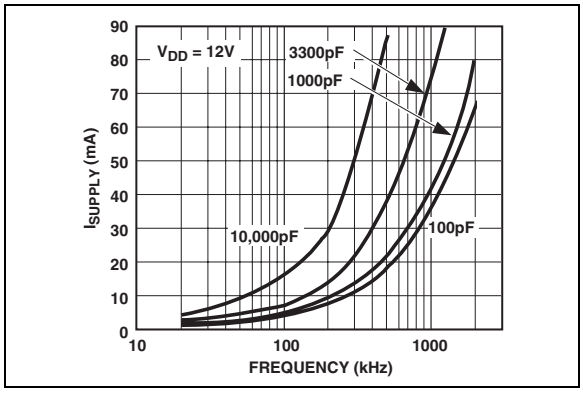


FIGURE 2-17: *Supply Current vs. Frequency.*

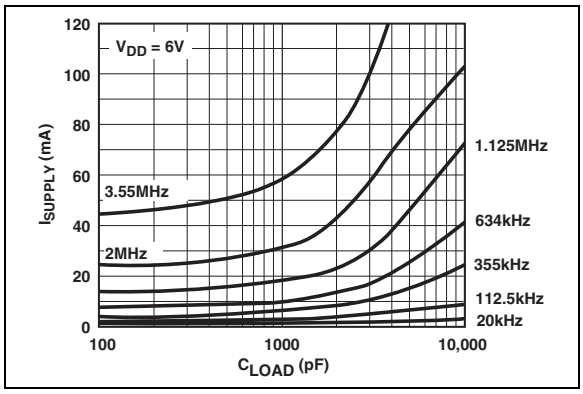


FIGURE 2-15: *Supply Current vs. Capacitive Load.*

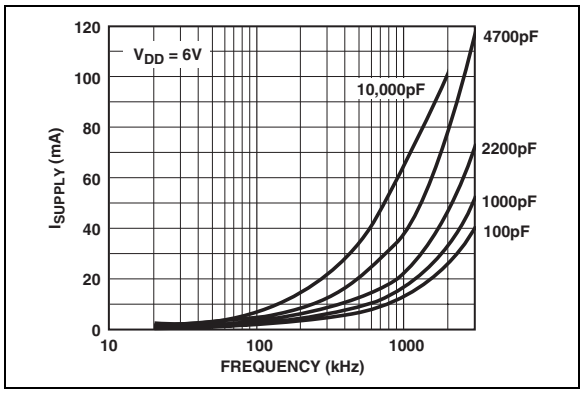
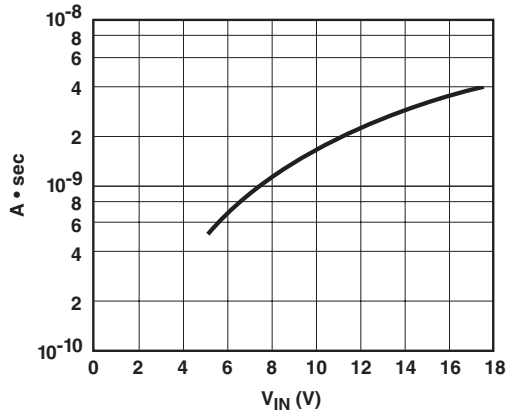


FIGURE 2-18: *Supply Current vs. Frequency.*

Typical Performance Curves (Continued)



Note: The values on this graph represent the loss seen by both drivers in a package during one complete cycle. For a single driver, divide the stated values by 2. For a single transition of a single driver, divide the stated value by 4.

FIGURE 2-19: *TC4423 Crossover Energy.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

8-Pin PDIP, CERDIP	16-Pin SOIC (Wide)	Symbol	Description
1	1	NC	No connect
2	2	IN A	Input A
—	3	NC	No connect
3	4	GND	Ground
—	5	GND	Ground
—	6	NC	No connect
4	7	IN B	Input B
—	8	NC	No connect
—	9	NC	No connect
5	10	OUT B	Output B
—	11	OUT B	Output B
6	12	V_{DD}	Supply input
—	13	V_{DD}	Supply input
7	14	OUT A	Output A
—	15	OUT A	Output A
8	16	NC	No connect

Note 1: Duplicate pins must be connected for proper operation.

3.1 Input A

Input A is a TTL/CMOS compatible input that controls Output A. This input has 300 mV of hysteresis between the high and low input levels that allows it to be driven from slow rising and falling signals and provide noise immunity.

3.2 Input B

Input B TTL/CMOS compatible input that controls Output B. This input has 300 mV of hysteresis between the high and low input levels that allows it to be driven from slow rising and falling signals and provide noise immunity.

3.3 Output B

Output B is a CMOS push-pull output that is capable of sourcing 3A peaks of current (V_{DD} = 18V) into a capacitive load. The low output impedance ensures the gate of the external MOSFET will stay in the intended state even during large transients. This output also has a reverse current latch-up rating of 1.5A.

3.4 Output A

Output A is a CMOS push-pull output that is capable of sourcing 3A peaks of current (V_{DD} = 18V) into a capacitive load. The low output impedance ensures the gate of the external MOSFET will stay in the intended state even during large transients. This output also has a reverse current latch-up rating of 1.5A.

3.5 Supply Input (V_{DD})

V_{DD} is the bias supply input for the MOSFET driver and has a voltage range of 4.5V to 18V. This input must be decoupled to ground with a local ceramic capacitor. This bypass capacitor provides a localized low-impedance path for the peak currents that are to be provided to the load.

3.6 Ground (GND)

Ground is the device return pin. The Ground pin(s) should have a low impedance connection to the bias supply source return. High peak currents will flow out the Ground pin(s) when the capacitive load is being discharged.

4.0 APPLICATIONS INFORMATION

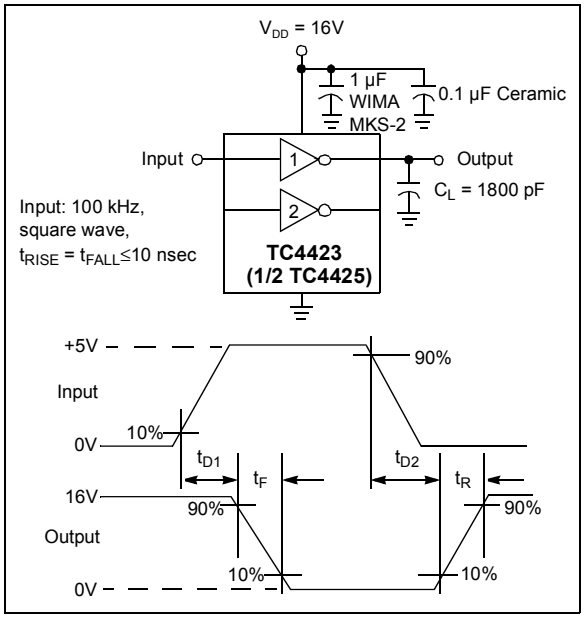


FIGURE 4-1: *Inverting Driver Switching Time.*

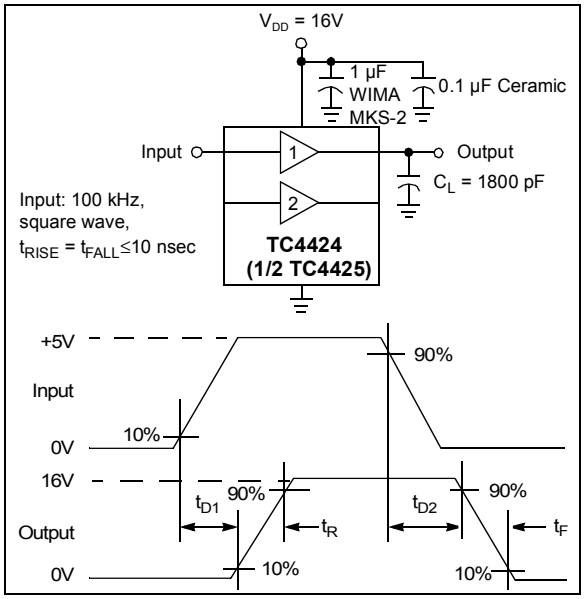
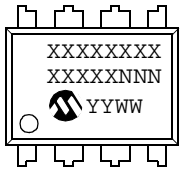


FIGURE 4-2: *Noninverting Driver Switching Time.*

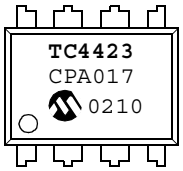
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

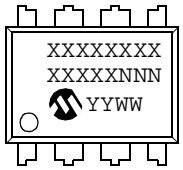
8-Lead PDIP (300 mil)



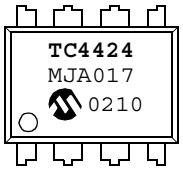
Example:



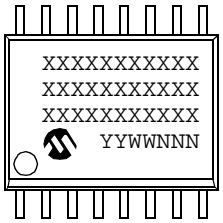
8-Lead CERDIP (300 mil)



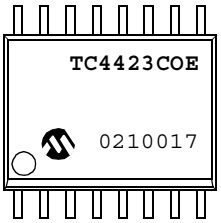
Example:



16-Lead SOIC (300 mil)



Example:

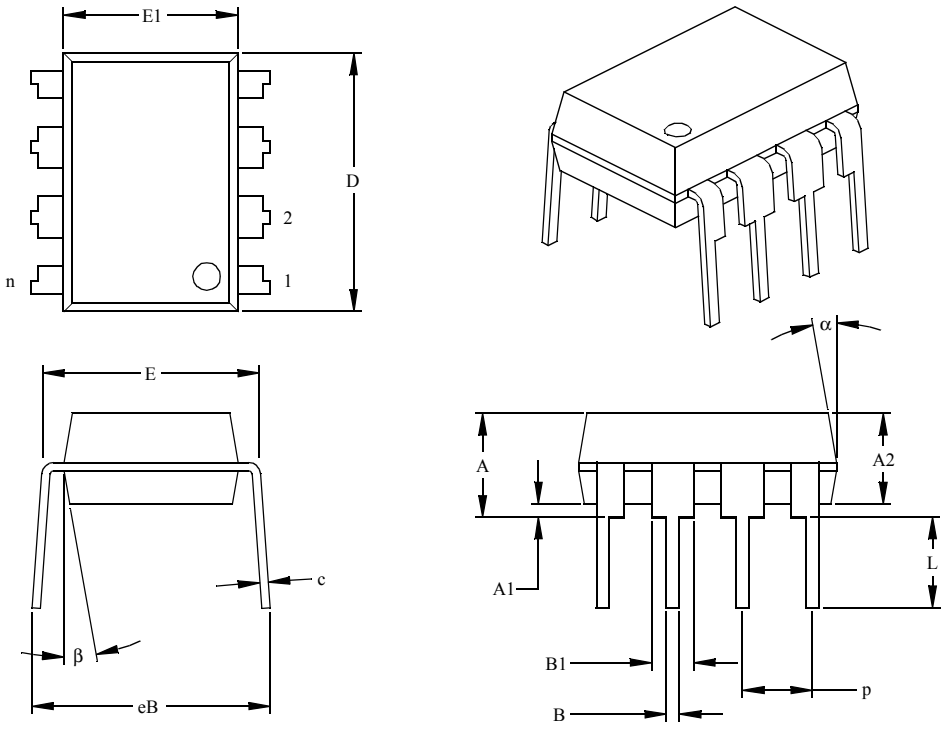


Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

***** Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code). For marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

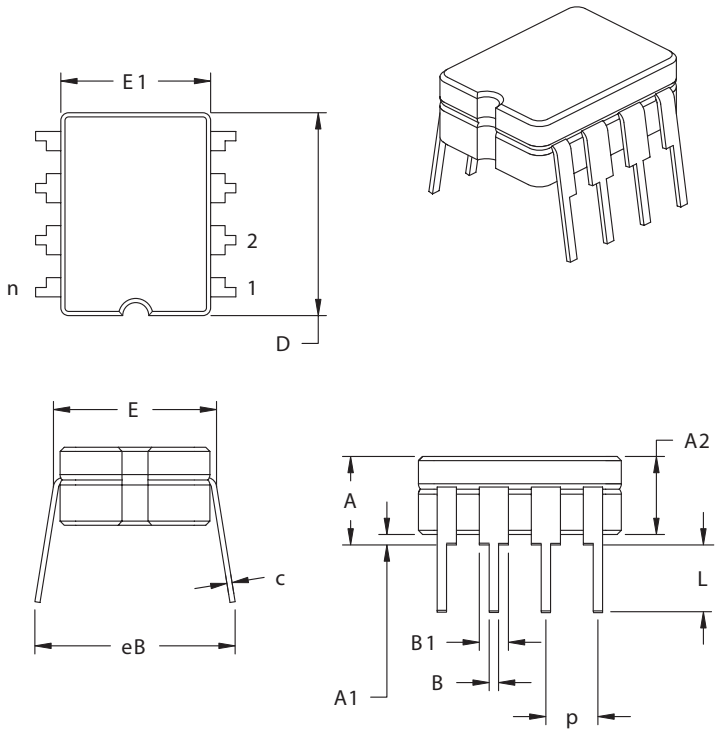


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Ceramic Dual In-line – 300 mil (CERDIP)



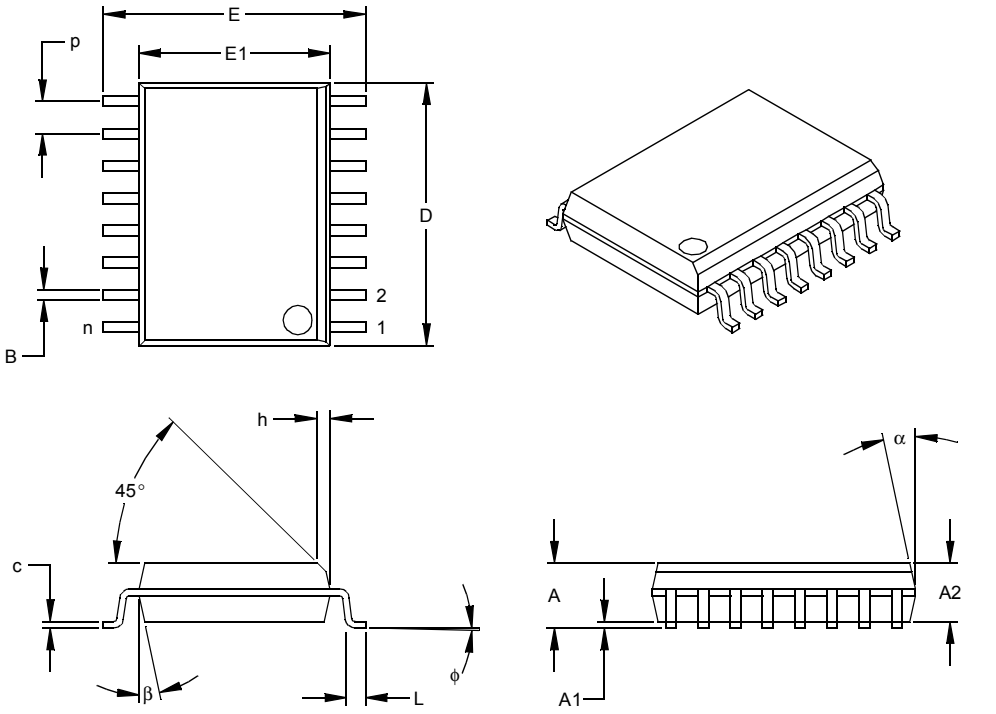
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.160	.180	.200	4.06	4.57	5.08
Standoff §	A1	.020	.030	.040	0.51	0.77	1.02
Shoulder to Shoulder Width	E	.290	.305	.320	7.37	7.75	8.13
Ceramic Pkg. Width	E1	.230	.265	.300	5.84	6.73	7.62
Overall Length	D	.370	.385	.400	9.40	9.78	10.16
Tip to Seating Plane	L	.125	.163	.200	3.18	4.13	5.08
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.055	.065	1.14	1.40	1.65
Lower Lead Width	B	.016	.018	.020	0.41	0.46	0.51
Overall Row Spacing	eB	.320	.360	.400	8.13	9.15	10.16

*Controlling Parameter

JEDEC Equivalent: MS-030

Drawing No. C04-010

16-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		16			16	
Pitch	p		.050			1.27	
Overall Height	A	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59
Overall Length	D	.398	.406	.413	10.10	10.30	10.49
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	ϕ	0	4	8	0	4	8
Lead Thickness	c	.009	.011	.013	0.23	0.28	0.33
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-013
Drawing No. C04-102

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	TC4423:	3A Dual MOSFET Driver, Inverting
	TC4424:	3A Dual MOSFET Driver, Non-Inverting
	TC4425:	3A Dual MOSFET Driver, Complementary
Temperature Range:	C =	0°C to +70°C
	E =	-40°C to +85°C
	M =	-55°C to +125°C (CERDIP only)
	V =	-40°C to +125°C (16-pin SOIC only)
Package:	PA =	Plastic DIP, (300 mil body), 8-lead
	JA =	Ceramic DIP, (300 mil body), 8-lead
	OE =	SOIC (Wide), 16-pin
	OE713 =	SOIC (Wide), 16-pin (Tape and Reel)

Examples:

a) TC4423COE: Commerical Temp., SOIC package.

b) TC4423CPA: Commercial Temp., PDIP package.

c) TC4423MJA: Military Temperature, Ceramic DIP package.

a) TC4424COE713: Tape and Reel, Commerical Temp., SOIC package.

b) TC4424EPA: Commercial Temp., PDIP package.

a) TC4425EOE: Extended Temperature, SOIC package.

b) TC4425CPA: Commercial Temp., PDIP package.

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
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3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200 Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: http://www.microchip.com

Rocky Mountain
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966 Fax: 480-792-4338

Atlanta
3780 Mansell Road, Suite 130
Alpharetta, GA 30022
Tel: 770-640-0034 Fax: 770-640-0307

Boston
2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848 Fax: 978-692-3821

Chicago
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas
4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423 Fax: 972-818-2924

Detroit
Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250 Fax: 248-538-2260

Kokomo
2767 S. Albright Road
Kokomo, Indiana 46902
Tel: 765-864-8360 Fax: 765-864-8387

Los Angeles
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

San Jose
Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto
6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Australia
Microchip Technology Australia Pty Ltd
Marketing Support Division
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing
Microchip Technology Consulting (Shanghai) Co., Ltd., Beijing Liaison Office
Unit 915
Bei Hai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Chengdu
Microchip Technology Consulting (Shanghai) Co., Ltd., Chengdu Liaison Office
Rm. 2401-2402, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-86766200 Fax: 86-28-86766599

China - Fuzhou
Microchip Technology Consulting (Shanghai) Co., Ltd., Fuzhou Liaison Office
Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506 Fax: 86-591-7503521

China - Hong Kong SAR
Microchip Technology Hongkong Ltd.
Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

China - Shanghai
Microchip Technology Consulting (Shanghai) Co., Ltd.
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

China - Shenzhen
Microchip Technology Consulting (Shanghai) Co., Ltd., Shenzhen Liaison Office
Rm. 1812, 18/F, Building A, United Plaza
No. 5022 Binhe Road, Futian District
Shenzhen 518033, China
Tel: 86-755-82901380 Fax: 86-755-82966626

China - Qingdao
Rm. B505A, Fullhope Plaza,
No. 12 Hong Kong Central Rd.
Qingdao 266071, China
Tel: 86-532-5027355 Fax: 86-532-5027205

India
Microchip Technology Inc.
India Liaison Office
Marketing Support Division
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan
Microchip Technology Japan K.K.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

Korea
Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Singapore
Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-6334-8870 Fax: 65-6334-8850

Taiwan
Microchip Technology (Barbados) Inc., Taiwan Branch
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Austria
Microchip Technology Austria GmbH
Durisolstrasse 2
A-4600 Wels
Austria
Tel: 43-7242-2244-399
Fax: 43-7242-2244-393

Denmark
Microchip Technology Nordic ApS
Regus Business Centre
Lautrup hoj 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France
Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - ler Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany
Microchip Technology GmbH
Steinheilstrasse 10
D-85737 Ismaning, Germany
Tel: 49-089-627-144-100
Fax: 49-089-627-144-44

Italy
Microchip Technology SRL
Via Quasimodo, 12
20025 Legnano (MI)
Milan, Italy
Tel: 39-0331-742611 Fax: 39-0331-466781

United Kingdom
Microchip Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

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