TDA9109/S

LOW-COST DEFLECTION PROCESSOR FOR MULTISYNC MONITORS

PRELIMINARY DATA

HORIZONTAL

- SELF-ADAPTATIVE
- DUAL PLL CONCEPT
- 150kHz MAXIMUM FREQUENCY
- X-RAY PROTECTION INPUT
- I^2C CONTROLS :
  HORIZONTAL DUTY-CYCLE, H-POSITION, FREE RUNNING FREQUENCY, FREQUENCY GENERATOR FOR BURN-IN MODE

VERTICAL

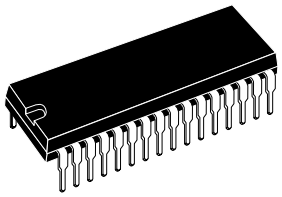
- VERTICAL RAMP GENERATOR
- 50 TO 185Hz AGC LOOP
- GEOMETRY TRACKING WITH VPOS & VAMP
- I^2C CONTROLS :
  VAMP, VPOS, S-CORR, C-CORR
- DC BREATHING COMPENSATION

I^2C GEOMETRY CORRECTIONS

- VERTICAL PARABOLA GENERATOR
  (Pin Cushion - E/W, Keystone, Corner)
- HORIZONTAL DYNAMIC PHASE
  (Side Pin Balance & Parallelogram)
- VERTICAL DYNAMIC FOCUS
  (Vertical Focus Amplitude)

GENERAL

- SYNC PROCESSOR
- 12V SUPPLY VOLTAGE
- 8V REFERENCE VOLTAGE
- HOR. & VERT. LOCK/UNLOCK OUTPUTS
- READ/WRITE I^2C INTERFACE
- HORIZONTAL AND VERTICAL MOIRE
- B+ REGULATOR
  - INTERNAL PWM GENERATOR FOR B+ CURRENT MODE STEP-UP CONVERTER
  - SOFT START
  - I^2C ADJUSTABLE B+ REFERENCE VOLTAGE
  - OUTPUT PULSES SYNCHRONIZED ON HORIZONTAL FREQUENCY
  - INTERNAL MAXIMUM CURRENT LIMITATION



SHRINK32
(Plastic Package)

ORDER CODE : TDA9109/S

- COMPARED WITH THE TDA9109, THE TDA9109/S HAS :
  - CORNER CORRECTION,
  - HORIZONTAL MOIRÉ,
  - B+ SOFT START,
  - INCREASED MAX. VERTICAL FREQUENCY,
  - NO HORIZONTAL FOCUS,
  - NO STEP DOWN OPTION FOR DC/DC CONVERTER.

DESCRIPTION

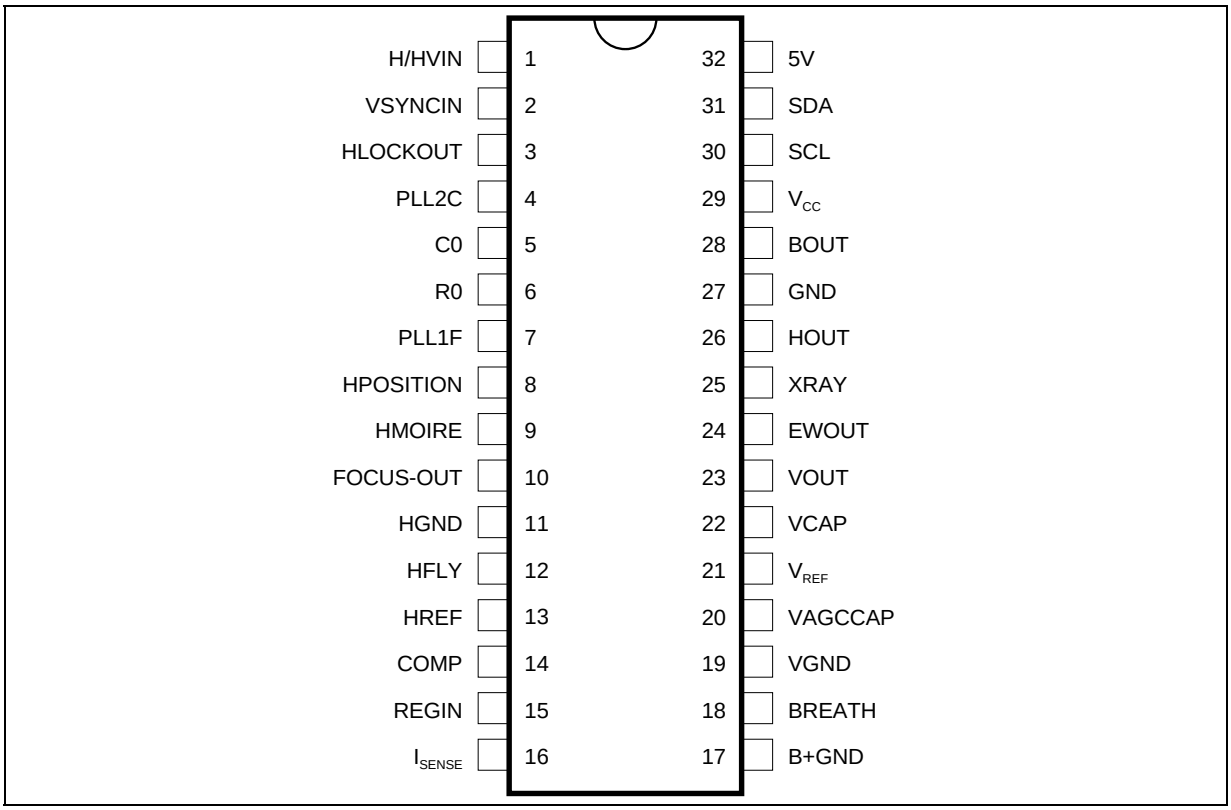
The TDA9109/S is a monolithic integrated circuit assembled in 32-pin shrink dual in line plastic package. This IC controls all the functions related to the horizontal and vertical deflection in multimode or multi-frequency computer display monitors.

The internal sync processor, combined with the very powerful geometry correction block make the TDA9109/S suitable for very high performance monitors, using very few external components.

The horizontal jitter level is very low. It is particularly well suited for high-end 15" and 17" monitors.

Combined with the ST7275 Microcontroller family, TDA9206 (Video preamplifier) and STV942x (On-Screen Display controller) the TDA9109/S allows fully I^2C bus controlled computer display monitors to be built with a reduced number of external components.

PIN CONNECTIONS



PIN CONNECTIONS

Pin	Name	Function
1	H/HVIN	TTL compatible Horizontal sync Input (separate or composite)
2	VSYNCIN	TTL compatible Vertical sync Input (for separated H&V)
3	HLOCKOUT	First PLL Lock/Unlock Output (0V unlocked - 5V locked)
4	PLL2C	Second PLL Loop Filter
5	C0	Horizontal Oscillator Capacitor
6	R0	Horizontal Oscillator Resistor
7	PLL1F	First PLL Loop Filter
8	HPOSITION	Horizontal Position Filter (capacitor to be connected to HGND)
9	HMOIRE	Horizontal Moiré Output (to be connected to PLL2C through a resistor divider)
10	FOCUSOUT	Vertical Dynamic Focus Output
11	HGND	Horizontal Section Ground
12	HFLY	Horizontal Flyback Input (positive polarity)
13	HREF	Horizontal Section Reference Voltage (to be filtered)
14	COMP	B+ Error Amplifier Output for frequency compensation and gain setting
15	REGIN	Regulation Input of B+ control loop
16	I_{SENSE}	Sensing of external B+ switching transistor current
17	B+GND	Ground (related to B+ reference adjustment)
18	BREATH	DC Breathing Input Control (compensation of vertical amplitude against EHV variation)
19	VGND	Vertical Section Ground
20	VAGCCAP	Memory Capacitor for Automatic Gain Control Loop in Vertical Ramp Generator
21	V_{REF}	Vertical Section Reference Voltage (to be filtered)
22	VCAP	Vertical Sawtooth Generator Capacitor
23	VOUT	Vertical Ramp Output (with frequency independant amplitude and S or C Corrections if any). It is mixed with vertical position voltage and vertical moiré.
24	EWOUT	Pin Cushion - E/W Correction Parabola Output
26	HOUT	Horizontal Drive Output (internal transistor, open collector)
25	XRAY	X-RAY protection input (with internal latch function)
27	GND	General Ground (referenced to V_{CC})
28	BOUT	B+ PWM Regulator Output
29	V_{CC}	Supply Voltage (12V typ)
30	SCL	I^2C Clock Input
31	SDA	I^2C Data Input
32	5V	Supply Voltage (5V typ.)

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QUICK REFERENCE DATA

Parameter	Value	Unit
Horizontal Frequency	15 to 150	kHz
Autosynch Frequency (for given R0 and C0)	1 to 4.5 f0	
± Horizontal Sync Polarity Input	YES	
Polarity Detection (on both Horizontal and Vertical Sections)	YES	
TTL Composite Sync	YES	
Lock/Unlock Identification (on both Horizontal 1st PLL and Vertical Section)	YES	
I^2C Control for H-Position	± 10	%
XRAY Protection	YES	
I^2C Horizontal Duty Cycle Adjust	30 to 60	%
I^2C Free Running Frequency Adjustment	0.8 to 1.3 f0	
Stand-by Function	YES	
Dual Polarity H-Drive Outputs	NO	
Supply Voltage Monitoring	YES	
PLL1 Inhibition Possibility	NO	
Blanking Outputs	NO	
Vertical Frequency	35 to 200	Hz
Vertical Autosync (for 150nF on Pin 22 and 470nF on Pin 20)	50 to 185	Hz
Vertical S-Correction	YES	
Vertical C-Correction	YES	
Vertical Amplitude Adjustment	YES	
DC Breathing Control on Vertical Amplitude	YES	
Vertical Position Adjustment	YES	
East/West (E/W) Parabola Output (also known as Pin Cushion Output)	YES	
E/W Correction Amplitude Adjustment	YES	
Keystone Adjustment	YES	
Corner Correction	YES	
Internal Dynamic Horizontal Phase Control	YES	
Side Pin Balance Amplitude Adjustment	YES	
Parallelogram Adjustment	YES	
Tracking of Geometric Corrections with Vertical Amplitude and Position	YES	
Reference Voltage (both on Horizontal and Vertical)	YES	
Vertical Dynamic Focus	YES	
I^2C Horizontal Dynamic Focus Amplitude Adjustment	NO	
I^2C Horizontal Dynamic Focus Symmetry Adjustment	NO	
I^2C Vertical Dynamic Focus Amplitude Adjustment	YES	
Detection of Input Sync Type	YES	
Vertical Moiré Output	YES	
Horizontal Moiré Output	YES	
I^2C Controlled Moiré Amplitude	YES	
Frequency Generator for Burn-in	YES	
Fast I^2C Read/Write	400	kHz
B+ Regulation adjustable by I^2C	YES	
B+ Soft Start	YES	

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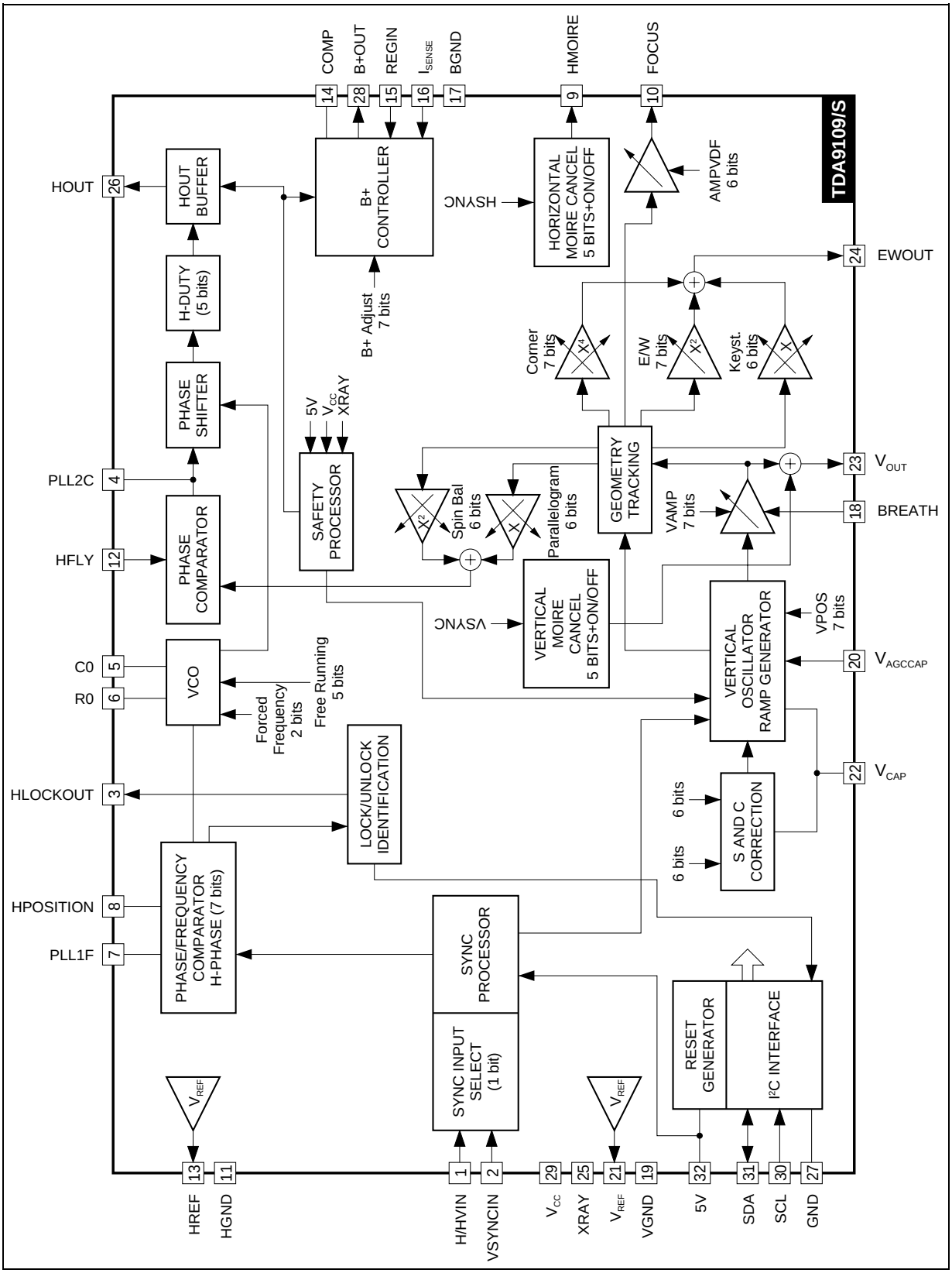
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (Pin 29)	13.5	V
V_{DD}	Supply Voltage (Pin 32)	5.7	V
V_{IN}	Max Voltage on Pin 4 Pin 5 Pins 6, 7, 8, 14, 15, 16, 20, 22 Pins 9, 10, 18, 23, 24, 25, 26, 28 Pins 1, 2, 3, 30, 31	4.0 6.4 8.0 V_{CC} V_{DD}	V V V V V
VESD	ESD susceptibility Human Body Model,100pF Discharge through 1.5kΩ EIAJ Norm, 200pF Discharge through 0Ω	2 300	kV V
T_{stg}	Storage Temperature	-40, +150	°C
T_j	Junction Temperature	+150	°C
T_{oper}	Operating Temperature	0, +70	°C

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THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Junction-Ambient Thermal Resistance	Max.	65	°C/W

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SYNC PROCESSOR

Operating Conditions (V_{DD} = 5V, T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
HsVR	Voltage on H/HVIN Input	Pin 1	0		5	V
MinD	Minimum Horizontal Input Pulses Duration	Pin 1	0.7			µs
Mduty	Maximum Horizontal Input Signal Duty Cycle	Pin 1			25	%
VsVR	Voltage on VSYNCIN	Pin 2	0		5	V
VSW	Minimum Vertical Sync Pulse Width	Pin 2	5			µs
VSmD	Maximum Vertical Sync Input Duty Cycle	Pin 2			15	%
VextM	Maximum Vertical Sync Width on TTL H/Vcomposite	Pin 1			750	µs
$I_{HLOCKOUT}$	Sink and Source Current	Pin3			250	µA

Electrical Characteristics (V_{DD} = 5V, T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VINTH	Horizontal and Vertical Input Logic Level (Pins 1, 2)	Low Level High Level	 2.2		0.8	V V
RIN	Horizontal and Vertical Pull-Up Resistor	Pins 1, 2		200		kΩ
TfrOut	Fall and Rise Time, Output CMOS Buffer	Pin 3, C_{OUT} = 20pF			200	ns
VHlock	Horizontal 1st PLL Lock Output Status (Pin 3)	Locked, $I_{LOCKOUT}$ = -250µA Unlocked, $I_{LOCKOUT}$ = +250µA	 4.4	0 5	0.5	V V
VoutT	Extracted Vsync Integration Time (% of T_H) on H/V Composite (see Note 1)	C0 = 820pF	26	35		%

Note 1 : T_H is the horizontal period.

I^2C READ/WRITE (see Note 2)

Electrical Characteristics (V_{DD} = 5V,T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I^2C PROCESSOR						
Fscl	Maximum Clock Frequency	Pin 30			400	kHz
Tlow	Low period of the SCL Clock	Pin 30	1.3			µs
Thigh	High period of the SCL Clock	Pin 30	0.6			µs
Vinth	SDA and SCL Input Threshold	Pins 30,31		2.2		V
VACK	Acknowledge Output Voltage on SDA input with 3mA	Pin 31			0.4	V

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Note 2 : See also I^2C Table Control and I^2C Sub Address Control.

HORIZONTAL SECTION
Operating Conditions

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCO						
$R_{0(Min.)}$	Minimum Oscillator Resistor	Pin 6	6			kΩ
$C_{0(Min.)}$	Minimum Oscillator Capacitor	Pin 5	390			pF
$F_{(Max.)}$	Maximum Oscillator Frequency				150	kHz
OUTPUT SECTION						
I12m	Maximum Input Peak Current	Pin 12			5	mA
HOI	Horizontal Drive Output Maximum Current	Pin 26, Sunk current			30	mA

Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY AND REFERENCE VOLTAGES						
V_{CC}	Supply Voltage	Pin 29	10.8	12	13.2	V
V_{DD}	Supply Voltage	Pin 32	4.5	5	5.5	V
I_{CC}	Supply Current	Pin 29		50		mA
I_{DD}	Supply Current	Pin 32		5		mA
V_{REF-H}	Horizontal Reference Voltage	Pin 13, I = -2mA	7.4	8	8.6	V
V_{REF-V}	Vertical Reference Voltage	Pin 21, I = -2mA	7.4	8	8.6	V
I_{REF-H}	Max. Sourced Current on V_{REF-H}	Pin 13			5	mA
I_{REF-V}	Max. Sourced Current on V_{REF-V}	Pin 21			5	mA
1st PLL SECTION						
HpolT	Delay Time for detecting polarity change (see Note 3)	Pin 1	0.75			ms
V_{VCO}	VCO Control Voltage (Pin 7)	V_{REF-H} = 8V f_0 f_H(Max.)		1.3 6.2		V V
Vcog	VCO Gain (Pin 7)	R_0 = 6.49kΩ, C_0 = 820pF, $dF/dV = 1/11R_0C_0$		17.1		kHz/V
Hph	Horizontal Phase Adjustment (see Note 4)	% of Horizontal Period		±10		%
Vbmin Vbtyp Vbmax	Horizontal Phase Setting Value (Pin 8) (see Note 4) Minimum Value Typical Value Maximum Value	Sub-Address 01 Byte x1111111 Byte x1000000 Byte x0000000		 2.8 3.4 4.0		 V V V
IPll1U IPll1L	PLL1 Filter Current Charge	PLL1 is Unlocked PLL1 is Locked		±140 ±1		µA mA
f_0	Free Running Frequency Sub-Address 02 - Byte xxx10000	R_0 = 6.49kΩ, C_0 = 820pF, $f_0 = 0.97/8R_0C_0$		22.8		kHz
df0/dT	Free Running Frequency Thermal Drift (No drift on external components) (see Note 5)			-150		ppm/C
f_0(Min.) f_0(Max.)	Free Running Frequency Adjustment Minimum Value Maximum Value	Sub-Address 02 Byte xxx11111 Byte xxx00000		 0.8 1.3		 f0 f0
CR	PLL1 Capture Range	R_0 = 6.49kΩ, C_0 = 820pF, from f_0+0.5kHz to 4.5f_0 f_0 adjsusted to 22.8kHz f_H(Min.) f_H(Max.)	 100		 23.5	 kHz kHz
FF	Forced Frequency FF1 Byte 11xxxxxx FF2 Byte 10xxxxxx	Sub-Address 02		2f0 3f0		

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Notes : 3. This delay is mandatory to avoid a wrong detection of polarity change in the case of a composite sync.
4. See Figure 10 for explanation of reference phase.
5. These parameters are not tested on each unit. They are measured during our internal qualification.

HORIZONTAL SECTION (continued)
Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
2nd PLL SECTION AND HORIZONTAL OUTPUT SECTION						
FBth	Flyback Input Threshold Voltage (Pin 12)		0.65	0.75		V
Hjit	Horizontal Jitter	At 31.4kHz		70		ppm
HDmin HDmax	Horizontal Drive Output Duty-Cycle (Pin 26) (see Note 6)	Sub-Address 00 Byte xxx11111 Byte xxx00000 (see Note 7)		 30 60		 % %
XRAYth	X-RAY Protection Input Threshold Voltage	Pin 25, see Note 8		8		V
Vphi2	Internal Clamping Levels on 2nd PLL Loop Filter (Pin 4)	Low Level High Level		1.6 4.0		V V
VSCinh	Threshold Voltage to Stop H-Out,V-Out, B-Out and Reset XRAY when V_{CC} < VSCinh (see Note 8)	Pin 29		7.5		V
VSDinh	Threshold Voltage to Stop H-Out,V-Out, B-Out and Reset XRAY when V_{DD} < VSDinh	Pin 32		4.0		V
HDvd	Horizontal Drive Output (low level)	Pin 26, I_{OUT} = 30mA			0.4	V
VERTICAL DYNAMIC FOCUS FUNCTION (positive parabola)						
HDFDC	Bottom DC Output Level	R_{LOAD} = 10kΩ, Pin 10		2		V
TDHDF	DC Output Voltage Thermal Drift (see Note 5)			200		ppm/C
AMPVDF	Vertical Dynamic Focus Parabola Amplitude with VAMP and VPOS Typical Min. Byte 000000 Typ. Byte 100000 Max. Byte 111111	Sub-Address 0F		 0 0.5 1		 V_{PP} V_{PP} V_{PP}
VDFAMP	Parabola Amplitude Function of VAMP (tracking between VAMP and VDF) with VPOS Typ. (see Figure 1 and Note 9)	Sub-Address 05 Byte 10000000 Byte 11000000 Byte 11111111		 0.6 1 1.5		 V_{PP} V_{PP} V_{PP}
VHDFKeyt	Parabola Asymetry Function of VPOS Control (tracking between VPOS and VDF) with VAMP Max.	Sub-Address 06 Byte x0000000 Byte x1111111		 0.52 0.52		 V_{PP} V_{PP}

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Notes : 5. These parameters are not tested on each unit. They are measured during our internal qualification.
6. Duty Cycle is the ratio between the output transistor OFF time and the period. The power transistor is controlled OFF when the output transistor is OFF.
7. Initial Condition for Safe Operation Start Up
8. See Figure 14.
9. S and C correction are inhibited so the output sawtooth has a linear shape.

VERTICAL SECTION
Operating Conditions

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
OUTPUTS SECTION						
VEWM	Maximum E/W Output Voltage	Pin 24			6.5	V
VEWm	Minimum E/W Output Voltage	Pin 24	1.8			V
R_{LOAD}	Minimum Load for less than 1% Vertical Amplitude Drift	Pin 20	65			MΩ

Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VERTICAL RAMP SECTION						
VRB	Voltage at Ramp Bottom Point	V_{REF-V} = 8V, Pin 22		2		V
VRT	Voltage at Ramp Top Point (with Sync)	V_{REF-V} = 8V, Pin 22		5		V
VRTF	Voltage at Ramp Top Point (without Sync)	Pin 22		VRT-0.1		V
VSTD	Vertical Sawtooth Discharge Time	Pin 22, C_{22} = 150nF		70		µs
VFRF	Vertical Free Running Frequency (see Note 10)	$C_{OSC\ (Pin\ 22)}$ = 150nF Measured on Pin22		100		Hz
ASFR	AUTO-SYNC Frequency (see Note 11)	C_{22} = 150nF ±5%	50		185	Hz
RAFD	Ramp Amplitude Drift Versus Frequency at Maximum Vertical Amplitude (see Note 5)	C_{22} = 150nF 50Hz < f and f < 185Hz		200		ppm/Hz
Rlin	Ramp Linearity on Pin 22 (see Note 10)	2.5V < V_{27} and V_{27} < 4.5V		0.5		%
VPOS	Vertical Position Adjustment Voltage (Pin23 - VOUT mean value)	Sub Address 06 Byte x0000000 Byte x1000000 Byte x1111111	 3.65	 3.2 3.5 3.8	 3.3 	 V V V
VOR	Vertical Output Voltage (peak-to-peak on Pin 23)	Sub Address 05 Byte x0000000 Byte x1000000 Byte x1111111	 3.5	 2.25 3 3.75	 2.5 	 V V V
VOI	Vertical Output Maximum Current (Pin 23)			±5		mA
dVS	Max Vertical S-Correction Amplitude (see Note 12) x0xxxxxx inhibits S-CORR x1111111 gives max S-CORR	Sub Address 07 $\Delta V/V_{PP}$ at TV/4 $\Delta V/V_{PP}$ at 3TV/4		 -4 +4		 % %
Ccorr	Vertical C-Corr Amplitude x0xxxxxx inhibits C-CORR	Sub Address 08 $\Delta V/V_{PP}$ @ TV/2 Byte x1000000 Byte x1100000 Byte x1111111		 -3 0 3		 % % %

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Notes : 5. These parameters are not tested on each unit. They are measured during our internal qualification.
10. With Register 07 at Byte x0xxxxxx (S correction is inhibited) and with Register 08 at Byte x0xxxxxx (C correction is inhibited), the sawtooth has a linear shape.
11. This is the frequency range for which the vertical oscillator will automatically synchronize, using a single capacitor value on Pin 22 and with a constant ramp amplitude.
12. TV is the vertical period.

VERTICAL SECTION (continued)
Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
East/West (E/W) FUNCTION						
EW_{DC}	DC Output Voltage with Typ. VPOS, Keystone and Corner inhibited	Pin 24, see Figure 2		2.5		V
$TDEW_{DC}$	DC Output Voltage Thermal Drift	See Note 13		100		ppm/C
EWpara	Parabola Amplitude with Max. VAMP, Typ. VPOS, Keystone and Corner inhibited	Subaddress 0A Byte 11111111 Byte 11000000 Byte 10000000		 1.7 0.85 0		 V_{PP} V_{PP} V_{PP}
EWtrack	Parabola Amplitude Function of VAMP Control (tracking between VAMP and E/W) with Typ. VPOS, Typ. E/W Amplitude, Keystone and Corner inhibited (see Note 10)	Subaddress 05 Byte 10000000 Byte 11000000 Byte 11111111		 0.30 0.55 0.85		 V_{PP} V_{PP} V_{PP}
KeyAdj	Keystone Adjustment Capability with Typ. VPOS, Corner and E/W inhibited and Max. Vertical Amplitude (see Note 10 and Figure 4)	Subaddress 09 Byte 1x000000 Byte 1x111111		 0.65 0.65		 V_{PP} V_{PP}
KeyTrack	Intrinsic Keystone Function of VPOS Control (tracking between VPOS and E/W) with Max. E/W Amplitude,Max. Vertical Amplitude and Corner inhibited (see Note 13 and Figure 2) A/B Ratio B/A Ratio	Subaddress 06 Byte x0000000 Byte x1111111		 0.52 0.52		
Corner	Corner Amplitude with Max. VAMP, Typ. VPOS, Keystone and E/W inhibited	Subaddress 0B Byte 11111111 Byte 11000000 Byte 10000000		 1.7 0 -1.7		 V_{PP} V_{PP} V_{PP}
INTERNAL DYNAMIC HORIZONTAL PHASE CONTROL						
SPBpara	Side Pin Balance Parabola Amplitude (Figure 3) with Max. VAMP, Typ. VPOS and Parallelogram inhibited (see Notes 10 & 14)	Subaddress 0D Byte x1111111 Byte x1000000		 +1.4 -1.4		 $\%T_H$ $\%T_H$
SPBtrack	Side Pin Balance Parabola Amplitude function of VAMP Control (tracking between VAMP and SPB) with Max. SPB, Typ. VPOS and Parallelogram inhibited (see Notes 10 & 14)	Subaddress 05 Byte 10000000 Byte 11000000 Byte 11111111		 0.5 0.9 1.4		 $\%T_H$ $\%T_H$ $\%T_H$
ParAdj	Parallelogram Adjustment Capability with Max. VAMP, Typ. VPOS and Max. SPB (see Notes 10 & 14)	Subaddress 0E Byte x1111111 Byte x1000000		 +1.4 -1.4		 $\%T_H$ $\%T_H$
Partrack	Intrinsic Parallelogram Function of VPOS Control (tracking between VPOS and DHPC) with Max. VAMP, Max. SPB and Parallelogram inhibited (see Notes 10 & 14) A/B Ratio B/A Ratio	Subaddress 06 Byte x0000000 Byte x1111111		 0.52 0.52		
VERTICAL MOIRE						
VMOIRE	Vertical Moiré (measured on VOUT : Pin 23)	Subaddress 0C Byte 01x11111		 6		 mV
BREATHING COMPENSATION						
BRRANG	DC Breathing Control Range (see Note 15)	V18	1		12	V
BRADj	Vertical Output Variation versus DC Breathing Control (Pin 23)	$V_{18} \geq V_{REF-V}$ V_{18} = 4V		0 -10		% %

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Notes : 10. With Register 07 at Byte x0xxxxxx (S correction is inhibited) and with Register 08 at Byte x0xxxxxx (C correction is inhibited), the sawtooth has a linear shape.
13. These parameters are not tested on each unit. They are measured during our internal qualification.
14. T_H is the horizontal period.
15. When not used the DC breathing control pin must be connected to 12V.

B+ SECTION
Operating Conditions

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
FeedRes	Minimum Feedback Resistor	Resistor between Pins 15 and 14	5			kΩ

Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
OLG	Error Amplifier Open Loop Gain	At low frequency (see Note 16)		85		dB
I_{COMP}	Sunk Current on Error Amplifier Output when BOUT is in safety condition	Pin 14 (see Figure 14)		0.5		mA
UGBW	Unity Gain Bandwidth	(see Note 13)		6		MHz
IRI	Regulation Input Bias Current	Current sourced by Pin 15 (PNP base)		0.2		µA
EAOI	Error Amplifier Output Current	Current sourced by Pin 14 Current sunk by Pin 14			0.5 2	mA mA
CSG	Current Sense Input Voltage Gain	Pin 16		3		
MCEth	Max Current Sense Input Threshold Voltage	Pin 16		1.2		V
ISI	Current Sense Input Bias Current	Current sourced by Pin 16 (PNP base)		1		µA
Tonmax	Maximum ON Time of the external power transistor	% of Horizontal period, f_0 = 27kHz (see Note 17)		100		%
B+OSV	B+ Output Saturation Voltage	V_{28} with I_{28} = 10mA		0.25		V
IV_{REF}	Internal Reference Voltage	On error amp (+) input for Subaddress 0B Byte 1000000		4.8		V
V_{REFADJ}	Internal Reference Voltage Adjustment Range	Byte 1111111 Byte 0000000		+20 -20		% %
t_{FB+}	Fall Time	Pin 28		100		ns

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Notes : 13. These parameters are not tested on each unit. They are measured during our internal qualification.
16. These parameters are not tested on each unit. They are measured during our internal qualification procedure which includes characterization on batches coming from corners of our processes and also temperature characterization.
17. The external power transistor is OFF during about 400ns.

Figure 1 : Vertical Dynamic Focus Function

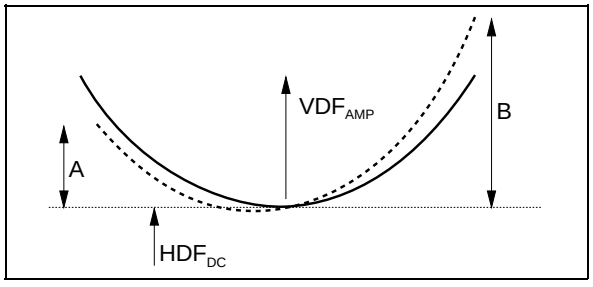

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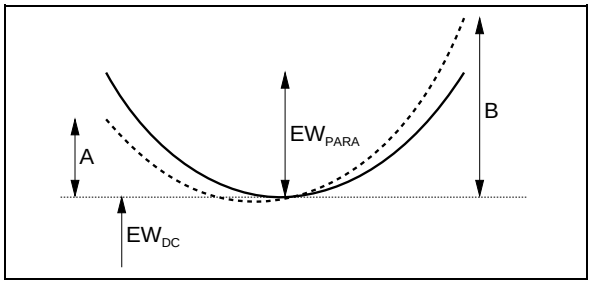
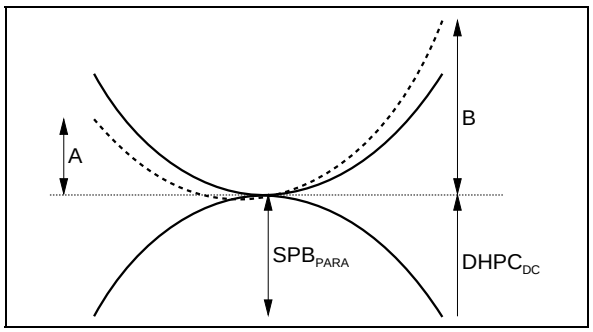
Figure 2 : E/W Output



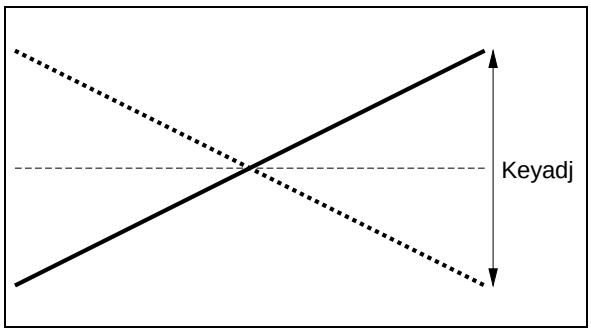
9109S-04.EPS

Figure 3 : Dynamic Horizontal Phase Control Output



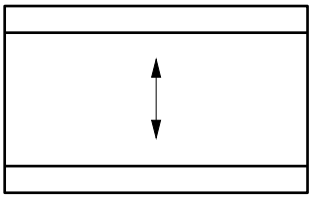
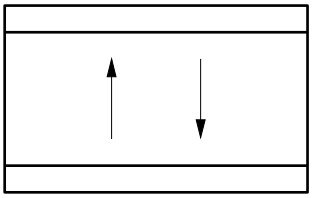
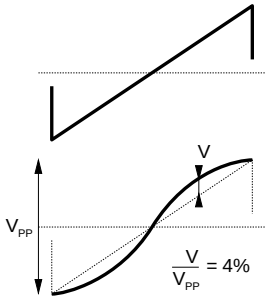
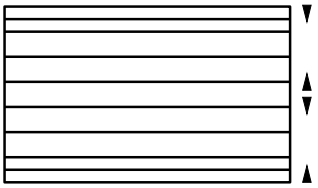
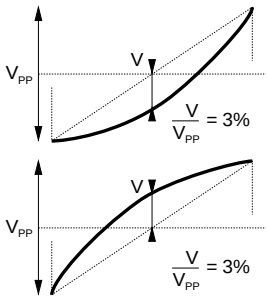
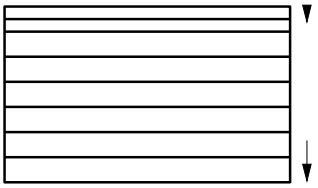
9109S-05.EPS

Figure 4 : Keystone Effect on E/W Output (PCC and Corner Inhibited)



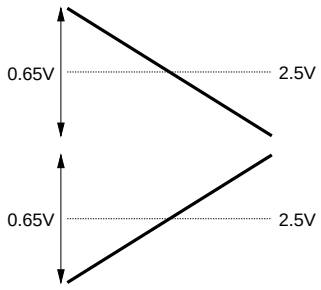
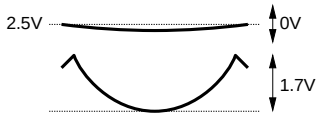
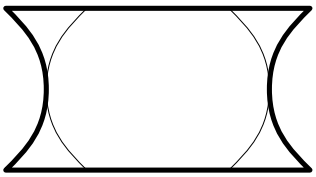
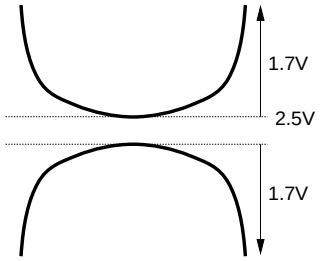
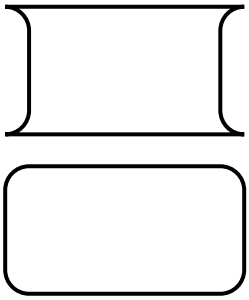
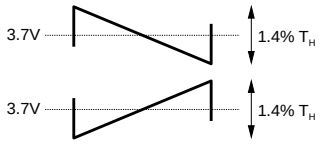
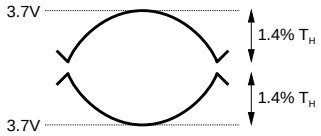
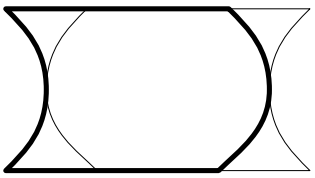
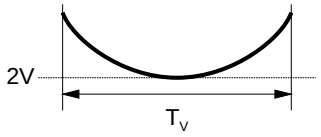
9109S-06.EPS

TYPICAL VERTICAL OUTPUT WAVEFORMS

Function	Sub Address	Pin	Byte	Specification	Effect on Screen
Vertical Size	05	23	10000000 11111111	V_{OUTDC} 2.25V V_{OUTDC} 3.75V	
Vertical Position DC Control	06	23	x0000000 x1000000 x1111111	V_{OUTDC} = 3.2V V_{OUTDC} = 3.5V V_{OUTDC} = 3.8V	
Vertical S Linearity	07	23	0xxxxxxx Inhibited 1x111111		
Vertical C Linearity	08	23	1x000000 1x111111		

9109S-06.TBL / 9109S-07.EPS TO 9109S-13.EPS

GEOMETRY OUTPUT WAVEFORMS

Function	Sub Address	Pin	Byte	Specification	Effect on Screen
Keystone (Trapezoid) Control	09	24	E/W+ Corner inhibited 1x000000 1x111111		
E/W (Pin Cushion) Control	0A	24	Keystone + Corner inhibited 10000000 11111111		
Corner Control	0B	24	Keystone+ E/W inhibited 11111111 10000000		
Parrallelogram Control	0E	Internal	SPB inhibited 1x000000 1x111111		
Side Pin Balance Control	0D	Internal	Parallelogram inhibited 1x000000 1x111111		
Vertical Dynamic Focus	0F	10			

9109S-07.TBL / 9109S-14.EPS TO 9109S-24.EPS

I²C BUS ADDRESS TABLE

Slave Address (8C) : Write Mode

Sub Address Definition

	D8	D7	D6	D5	D4	D3	D2	D1	
0	0	0	0	0	0	0	0	0	Horizontal Drive Selection / Horizontal Duty Cycle
1	0	0	0	0	0	0	0	1	Horizontal Position
2	0	0	0	0	0	0	1	0	Forced Frequency / Free Running Frequency
3	0	0	0	0	0	0	1	1	Sync Priority / Horizontal Moiré Amplitude
4	0	0	0	0	0	1	0	0	Refresh / B+ Reference Adjustment
5	0	0	0	0	0	1	0	1	Vertical Ramp Amplitude
6	0	0	0	0	0	1	1	0	Vertical Position Adjustment
7	0	0	0	0	0	1	1	1	S Correction
8	0	0	0	0	1	0	0	0	C Correction
9	0	0	0	0	1	0	0	1	E/W Keystone
A	0	0	0	0	1	0	1	0	E/W Amplitude
B	0	0	0	0	1	0	1	1	E/W Corner Adjustment
C	0	0	0	0	1	1	0	0	Vertical Moiré Amplitude
D	0	0	0	0	1	1	0	1	Side Pin Balance
E	0	0	0	0	1	1	1	0	Parallelogram
F	0	0	0	0	1	1	1	1	Vertical Dynamic Focus Amplitude

Slave Address (8D) : Read Mode

No sub address needed.

I²C BUS ADDRESS TABLE (continued)

	D8	D7	D6	D5	D4	D3	D2	D1
WRITE MODE								
00		HDrive 0, off [1], on		Horizontal Duty Cycle				
				[0]	[0]	[0]	[0]	[0]
01	Xray 1, reset [0]	Horizontal Phase Adjustment						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
02	Forced Frequency			Free Running Frequency				
	1, on [0], off	1, f0 x 2 [0], f0 x 3		[0]	[0]	[0]	[0]	[0]
03	Sync 0, Comp [1], Sep	HMoiré 1, on [0]		Horizontal Moiré Amplitude				
				[0]	[0]	[0]	[0]	[0]
04	Detect Refresh [0], off	B+ Reference Adjustment						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
05	Vramp 0, off [1], on	Vertical Ramp Amplitude Adjustment						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
06		Vertical Position Adjustment						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
07	S Select 1, on [0]		S Correction					
			[1]	[0]	[0]	[0]	[0]	[0]
08	C Select 1, on [0]		C Correction					
			[1]	[0]	[0]	[0]	[0]	[0]
09	E/W Key 0, off [1]		E/W Keystone					
			[1]	[0]	[0]	[0]	[0]	[0]
0A		E/W Amplitude						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
0B	E/W Cor 0, off [1]	E/W Corner Adjustment						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
0C	Test V 1, on [0], off	VMoiré 1, on [0]		Vertical Moiré Amplitude				
				[0]	[0]	[0]	[0]	[0]
0D	SPB Sel 0, off [1]		Side Pin Balance					
			[1]	[0]	[0]	[0]	[0]	[0]
0E	Parallelo 0, off [1]		Parallelogram					
			[1]	[0]	[0]	[0]	[0]	[0]
0F	Test H 1, on [0], off		Vertical Dynamic Focus Amplitude					
			[1]	[0]	[0]	[0]	[0]	[0]

READ MODE

	Hlock 0, on [1], no	Vlock 0, on [1], no	Xray 1, on [0], off	Polarity Detection		Sync Detection		
				H/V pol [1], negative	V pol [1], negative	Vext det [0], no det	H/V det [0], no det	V det [0], no det

[ ] initial value

Data is transferred with vertical sawtooth retrace.

We recommend to set the unspecified bit to [0] in order to assure the compatibility with future devices.

OPERATING DESCRIPTION

I - GENERAL CONSIDERATIONS

I.1 - Power Supply

The typical values of the power supply voltages V_{CC} and V_{DD} are 12V and 5V respectively. Optimum operation is obtained for V_{CC} between 10.8 and 13.2V and V_{DD} between 4.5 and 5.5V.

In order to avoid erratic operation of the circuit during the transient phase of V_{CC} and V_{DD} switching on, or off, the value of V_{CC} and V_{DD} are monitored : if V_{CC} is less than 7.5V typ. or if V_{DD} is less than 4.0V typ., the outputs of the circuit are inhibited.

Similarly, before V_{DD} reaches 4V, all the I^2C register are reset to their default value.

In order to have very good power supply rejection, the circuit is internally supplied by several voltage references (typ. value : 8V). Two of these voltage references are externally accessible, one for the vertical and one for the horizontal part. They can be used to bias external circuitry (if I_{LOAD} is less than 5mA). It is necessary to filter the voltage references by external capacitors connected to ground, in order to minimize the noise and consequently the "jitter" on vertical and horizontal output signals.

I.2 - I^2C Control

TDA9109/S belongs to the I^2C controlled device family. Instead of being controlled by DC voltages on dedicated control pins, each adjustment can be done via the I^2C Interface.
The I^2C bus is a serial bus with a clock and a data input. The general function and the bus protocol are specified in the Philips-bus data sheets.
The interface (Data and Clock) is a comparator with hysteresis ; the thresholds (less then 2.2V on rising edge, more than 0.8V on falling edge with 5V supply) are TTL-compatible. Spikes of up to 50ns are filtered by an integrator and the maximum clock speed is limited to 400kHz.
The data line (SDA) can be used bidirectionally. In read-mode the IC sends reply information (1 byte) to the micro-processor.
The bus protocol prescribes a full-byte transmission in all cases. The first byte after the start condition is used to transmit the IC-address (hexa 8C for write, 8D for read).

I.3 - Write Mode

In write mode the second byte sent contains the subaddress of the selected function to adjust (or controls to affect) and the third byte the corresponding data byte. It is possible to send more than one data byte to the IC. If after the third byte no stop or start condition is detected, the circuit increments automatically by one the momentary subaddress in the subaddress counter (auto-increment mode). So it is possible to transmit immediately the following data bytes without sending the IC address or subaddress. This can be useful to reinitialize all the controls very quickly (flash manner). This procedure can be finished by a stop condition.

The circuit has 16 adjustment capabilities : 3 for the horizontal part, 4 for the vertical, 2 for the E/W correction, 2 for the dynamic horizontal phase control,1 for the Moiré option, 3 for the horizontal and the vertical dynamic focus and 1 for the B+ reference adjustment.

17 bits are also dedicated to several controls (ON/OFF, Horizontal Forced Frequency, Sync Priority, Detection Refresh and XRAY reset).

I.4 - Read Mode

During the read mode the second byte transmits the reply information.

The reply byte contains the horizontal and vertical lock/unlock status, the XRAY activation status and, the horizontal and vertical polarity detection. It also contains the sync detection status which is used by the MCU to assign the sync priority.

A stop condition always stops all the activities of the bus decoder and switches to high impedance both the data and clock line (SDA and SCL).

See I^2C subaddress and control tables.

I.5 - Sync Processor

The internal sync processor allows the TDA9109/S to accept :
- separated horizontal & vertical TTL-compatible sync signal,
- composite horizontal & vertical TTL-compatible sync signal.

OPERATING DESCRIPTION (continued)

I.6 - Sync Identification Status

The MCU can read (address read mode : 8D) the status register via the I^2C bus, and then select the sync priority depending on this status.

Among other data this register indicates the presence of sync pulses on H/HVIN, VSYNCIN and (when 12V is supplied) whether a Vext has been extracted from H/HVIN. Both horizontal and vertical sync are detected even if only 5V is supplied.

In order to choose the right sync priority the MCU may proceed as follows (see I^2C Address Table) :
- refresh the status register,
- wait at least for 20ms (Max. vertical period),
- read this status register.

Sync priority choice should be :

Vext det	H/V det	V det	Sync priority Subaddress 03 (D8)	Comment Sync type
No	Yes	Yes	1	Separated H & V
Yes	Yes	No	0	Composite TTL H&V

Of course, when the choice is made, we can refresh the sync detections and verify that the extracted Vsync is present and that no sync type change has occured. The sync processor also gives sync polarity information.

I.7 - IC status

The IC can inform the MCU about the 1st horizontal PLL and vertical section status (locked or not) and about the XRAY protection (activated or not).
Resetting the XRAY internal latch can be done either by decreasing the V_{CC} or V_{DD} supply or directly resetting it via the I^2C interface.

I.8 - Sync Inputs

Both H/HVIN and VSYNCIN inputs are TTL compatible triggers with hysterisis to avoid erratic detection. Both inputs include a pull up resistor connected to V_{DD}.

I.9 - Sync Processor Output

The sync processor indicates on the HLOCKOUT Pin whether 1st PLL is locked to an incoming horizontal sync. HLOCKOUT is a TTL compatible CMOS output. Its level goes to high when locked. In the same time the D8 bit of the status register is set to 0.

This information is mainly used to trigger safety procedures (like reducing B+ value) as soon as a change is detected on the incoming sync. Further to this, it may be used in an automatic procedure for free running frequency (f0) adjustment :
Sending the desired f0 on the sync input and progressively decreasing the free running frequency I^2C register value (address 02), the HLOCKOUT Pin will go high as soon as the proper setting is reached.

Setting the free running frequency this way allows to fully exploit the TDA9109/S horizontal frequency range.

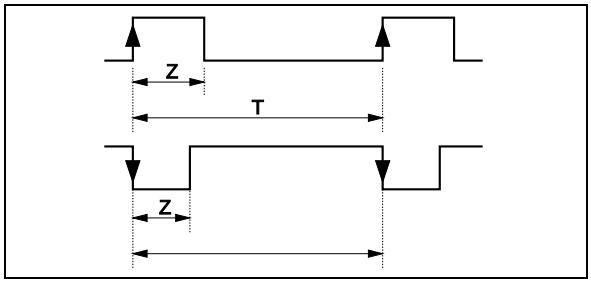
II - HORIZONTAL PART

II.1 - Internal Input Conditions

A digital signal (horizontal sync pulse or TTL composite) is sent by the sync processor to the horizontal input. It may be positive or negative (see Figure 5).

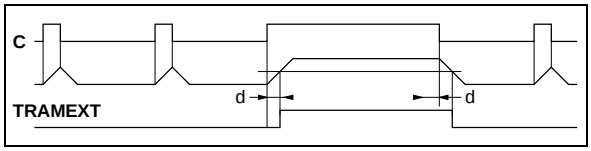
Using internal integration, both signals are recognized if Z/T < 25%. Synchronization occurs on the leading edge of the internal sync signal. The minimum value of Z is 0.7µs.

Figure 5



Another integration is able to extract the vertical pulse from composite sync if the duty cycle is higher than 25% (typically d = 35%) (see Figure 6).

Figure 6



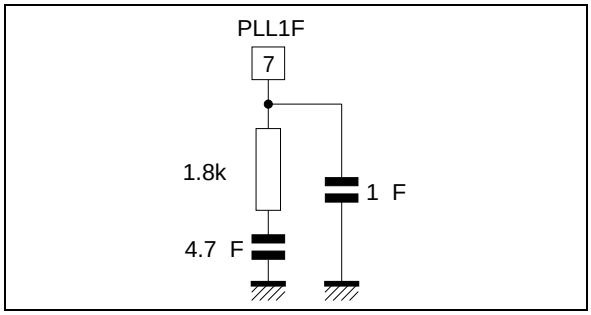
The last feature performed is the removal of equalization pulses to avoid parasitic pulses on the phase comparator (which would be disturbed by missing or extraneous pulses).

OPERATING DESCRIPTION (continued)

II.2 - PLL1

The PLL1 consists of a phase comparator, an external filter and a voltage-controlled oscillator (VCO).
The phase comparator is a "phase frequency" type designed in CMOS technology. This kind of phase detector avoids locking on wrong frequencies. It is followed by a "charge pump", composed of two current sources : sunk and sourced (typically I = 1mA when locked and I = 140µA when unlocked). This difference between lock/unlock allows smooth catching of the horizontal frequency by PLL1. This effect is reinforced by an internal original slow down system when PLL1 is locked, avoiding the horizontal frequency changing too quickly.
The dynamic behaviour of PLL1 is fixed by an external filter which integrates the current of the charge pump. A "CRC" filter is generally used (see Figure 7).
The PLL1 is internally inhibited during extracted vertical sync (if any) to avoid taking in account missing pulses or wrong pulses on phase comparator.The inhibition is done by a switch located between the charge pump and the filter (see Figure 8).
The VCO uses an external RC network. It delivers a linear sawtooth obtained by the charge and the discharge of the capacitor, with a current proportional to the current in the resistor. The typical

Figure 7



thresholds of the sawtooth are 1.6V and 6.4V.
The control voltage of the VCO is between 1.33V and 6V (see Figure 9). The theorical frequency range of this VCO is in the ratio of 1 to 4.5. The effective frequency range has to be smaller (1 to 4.2) due to clamp intervention on the filter lowest value. To remove the device and external components spread, it is possible to adjust the free running frequency through I^2C. This adjustment can be done automatically on the manufacturing line without manual operation by using Hlock/unlock information. The adjustment range is 0.8 to 1.3 f0 (where 1.3 f0 is the free running frequency at power on reset).

Figure 8 : Block Diagram

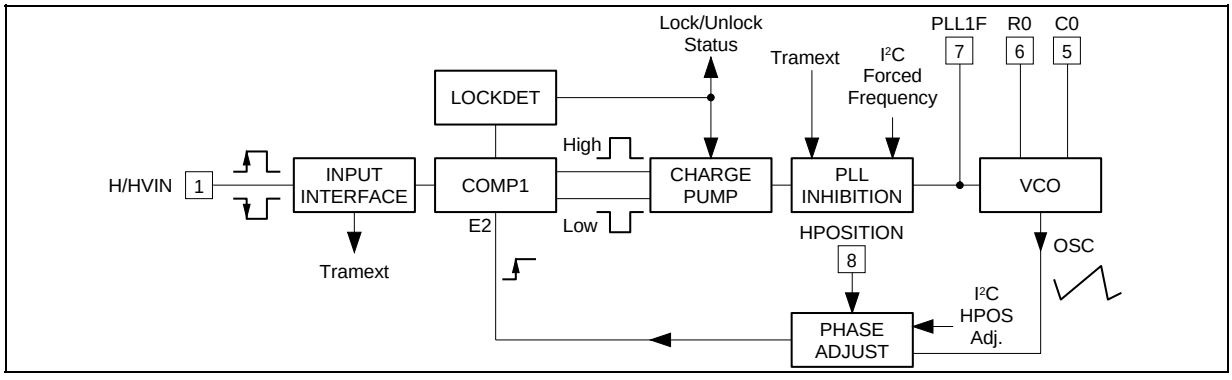
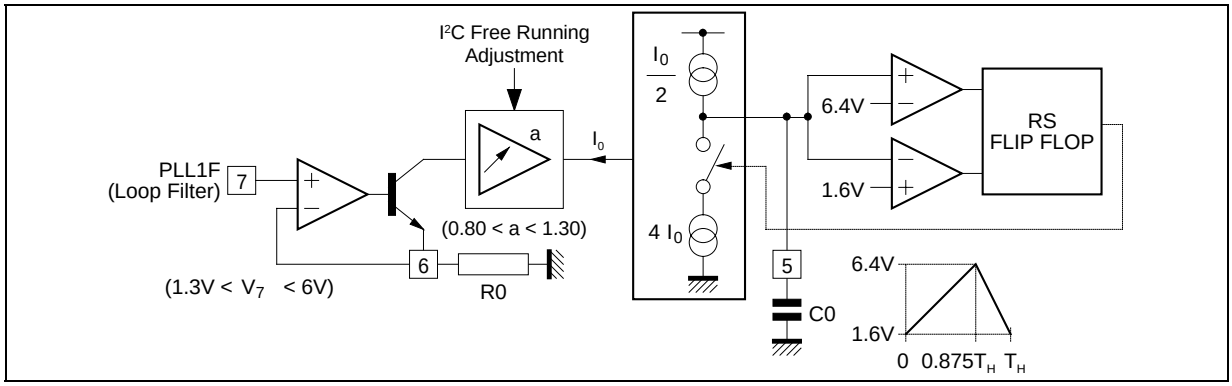


Figure 9 : Details of VCO



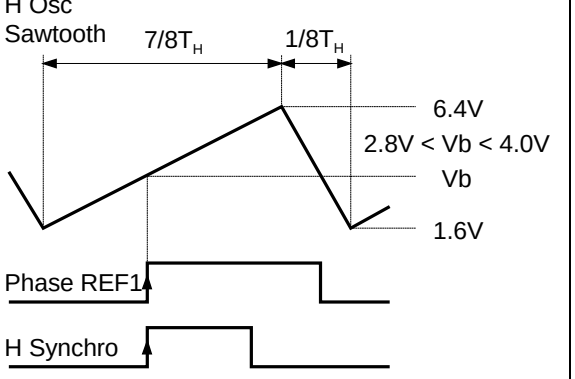
OPERATING DESCRIPTION (continued)

The sync frequency must always be higher than the free running frequency. For example, when using a sync range between 24kHz and 100kHz, the suggested free running frequency is 23kHz.

Another feature is the capability for the MCU to force the horizontal frequency through I^2C to 2xf0 or 3xf0 (for burn-in mode or safety requirements). In this case, the inhibition switch is opened, leaving PLL1 free, but the voltage on PLL1 filter is forced to 2.66V (for 2xf0) or 4.0V (for 3xf0).

PLL1 ensures the coincidence between the leading edge of the sync signal and a phase reference obtained by comparison between the sawtooth of the VCO and an internal DC voltage which is I^2C adjustable between 2.8V and 4.0V (corresponding to ± 10%) (see Figure 10).

Figure 10 : PLL1 Timing Diagram



Phase REF1 is obtained by comparison between the sawtooth and a DC voltage adjustable between 2.8V and 4.0V. The PLL1 ensures the exact coincidence between the signal phase REF and HSYNC. A ± T_H/10 phase adjustment is possible.

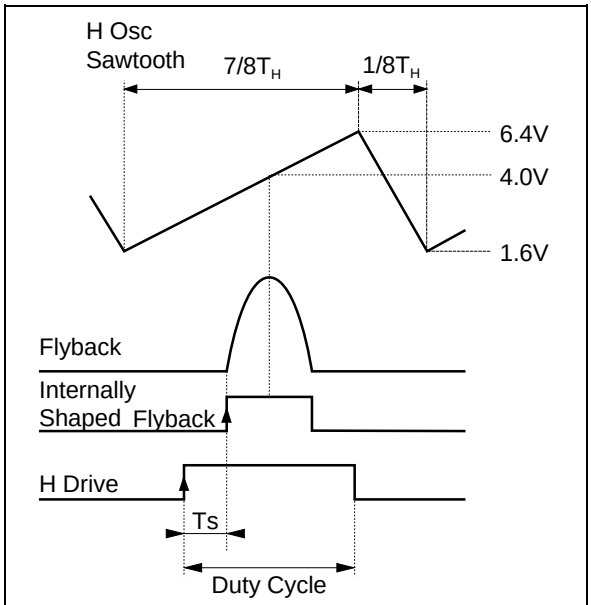
9109S-30.EPS

The TDA9109/S also includes a Lock/Unlock identification block which senses in real time whether PLL1 is locked or not on the incoming horizontal sync signal. The resulting information is available on HLOCKOUT (see Sync Processor).
When PLL1 is unlocked, it forces HLOCKOUT to high level.
The lock/unlock information is also available through the I^2C read.

II.3 - PLL2

PLL2 ensures a constant position of the shaped flyback signal in comparison with the sawtooth of the VCO, taking into account the saturation time Ts (see Figure 11).

Figure 11 : PLL2 Timing Diagram



The duty cycle of H-drive is adjustable between 30% and 60%.

9109S-31.EPS

The phase comparator of PLL2 (phase type comparator) is followed by a charge pump (typical output current : 0.5mA).

The flyback input consists of an NPN transistor. This input must be current driven. The maximum recommended input current is 5mA (see Figure 12).

The duty cycle is adjustable through I^2C from 30% to 60%. For start-up safe operation, the initial duty cycle (after power-on reset) is 60% in order to avoid having a too long conduction period of the horizontal scanning transistor.

The maximum storage time (Ts Max.) is ($0.44T_H$ - $T_{FLY}/2$). Typically, T_{FLY}/T_H is around 20% which means that Ts max is around 34% of T_H.

OPERATING DESCRIPTION (continued)

II.4 - Output Section

The H-drive signal is sent to the output through a shaping stage which also controls the H-drive duty cycle (I^2C adjustable) (see Figure 11). In order to secure the scanning power part operation, the output is inhibited in the following cases :
- when V_{CC} or V_{DD} are too low,
- when the XRAY protection is activated,
- during the Horizontal flyback,
- when the HDrive I^2C bit control is off.

The output stage consists of a NPN bipolar transistor. Only the collector is accessible (see Figure 13).

This output stage is intended for "reverse" base control, where setting the output NPN in off-state will control the power scanning transistor in off-state (see Application Diagram).
The maximum output current is 30mA, and the corresponding voltage drop of the output V_{CEsat} is 0.4V Max.
Obviously the power scanning transistor cannot be directly driven by the integrated circuit. An interface has to be added between the circuit and the power transistor either of bipolar or MOS type.

II.5 - X-RAY Protection

The X-Ray protection is activated by application of a high level on the X-Ray input (8V on Pin 25).
It inhibits the H-Drive and B+ outputs.
This protection is latched ; it may be reset either by V_{CC} or V_{DD} switch off or by I^2C (see Figure 14).

Figure 12 : Flyback Input Electrical Diagram

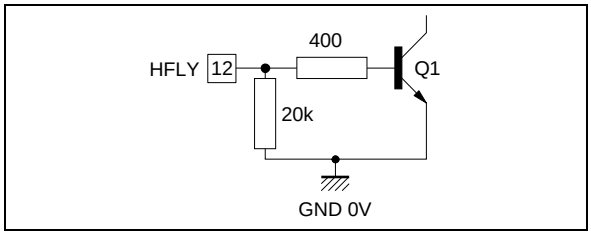
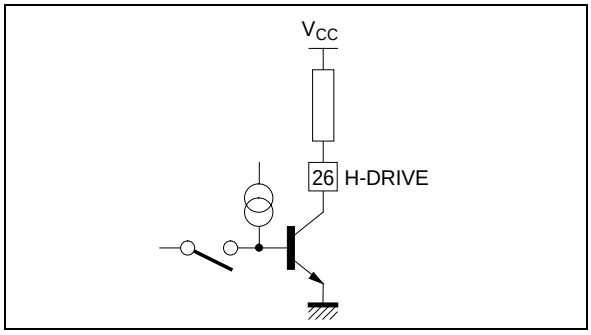


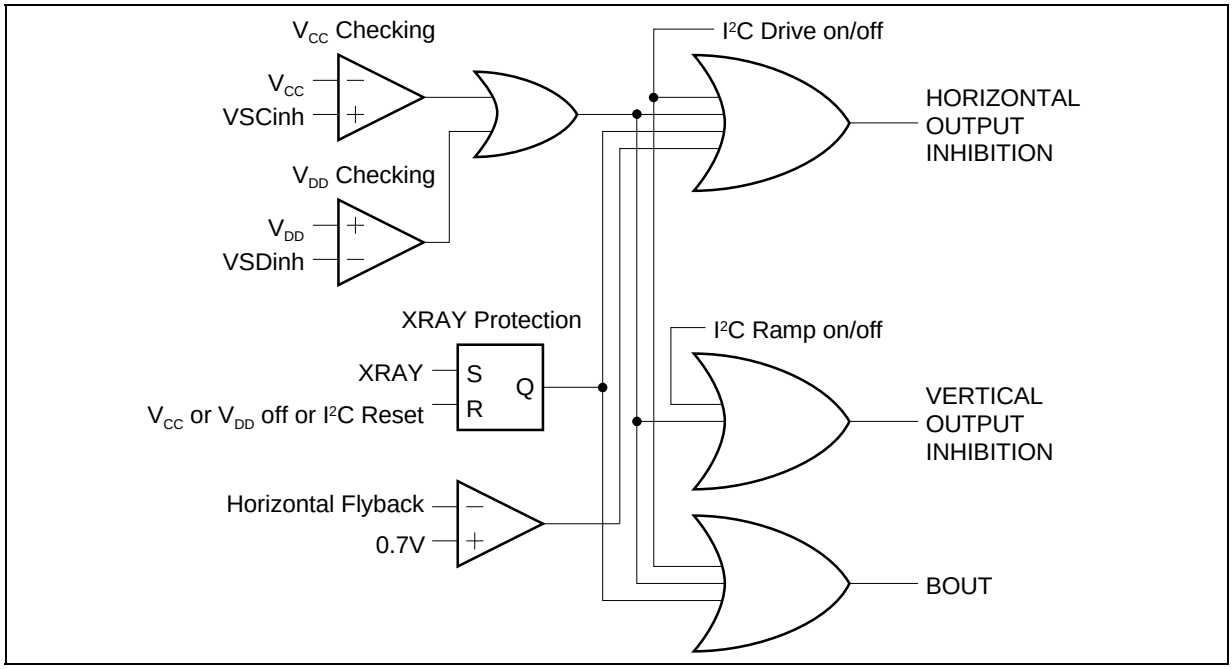
Figure 13



II.6 - Vertical Dynamic Focus

The TDA9109/S delivers a vertical parabola waveform on Pin 10.
This vertical dynamic focus is tracked with VPOS and VAMP. Its amplitude can be adjusted. It is also affected by S and C corrections. This positive signal once amplified is to be sent to the CRT focusing grids.

Figure 14 : Safety Functions Block Diagram



OPERATING DESCRIPTION (continued)

III - VERTICAL PART

III.1 - Function

When the synchronization pulse is not present, an internal current source sets the free running frequency. For an external capacitor, C_{OSC} = 150nF, the typical free running frequency is 100Hz.

The typical free running frequency can be calculated by :

$$f_0\,(Hz) = 1.5 \cdot 10^{-5} \cdot \frac{1}{C_{OSC}}$$

A negative or positive TTL level pulse applied on Pin 2 (VSYNC) as well as a TTL composite sync on Pin 1 can synchronize the ramp in the range [fmin , fmax]. This frequency range depends on the external capacitor connected on Pin 22. A 150nF (±5%) capacitor is recommended for 50Hz to 185Hz applications.

The typical maximum and minimum frequency, at 25°C and without any correction (S correction or C correction), can be calculated by :

$f_{(Max.)} = 3.5 \times f_0$ and $f_{(Min.)} = 0.33 \times f_0$

If S or C corrections are applied, these values are slighty affected.

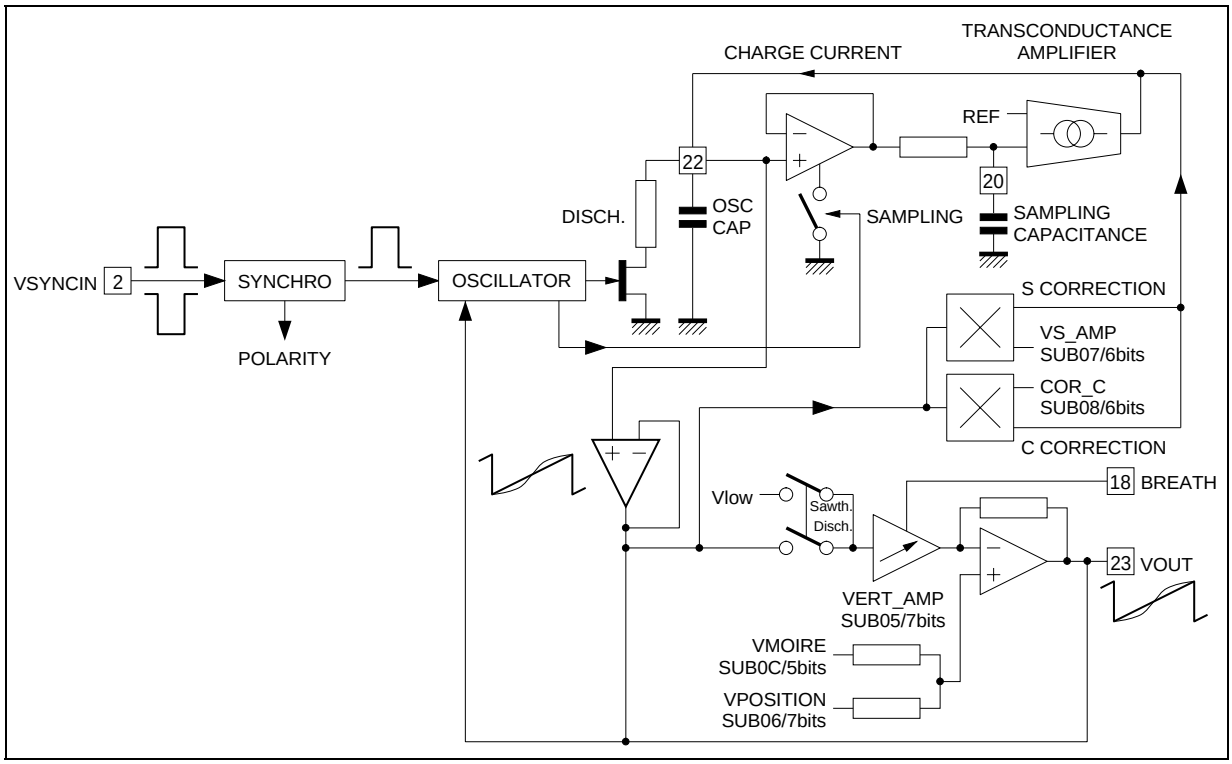
If a synchronization pulse is applied, the internal oscillator is synchonized immediately but its amplitude changes. An internal correction then adjusts it in less than half a second. The top value of the ramp (Pin 22) is sampled on the AGC capacitor (Pin 20) at each clock pulse and a transconductance amplifier modifies the charge current of the capacitor in such a way to make the amplitude again constant.

The read status register provides the vertical Lock-Unlock and the vertical sync polarity information.

We recommend the use of an AGC capacitor with low leakage current. A value lower than 100nA is mandatory.

A good stability of the internal closed loop is reached by a 470nF ± 5% capacitor value on Pin 20 (VAGC).

Figure 15 : AGC Loop Block Diagram



OPERATING DESCRIPTION (continued)

III.2 - I²C Control Adjustments

S and C correction shapes can then be added to this ramp. These frequency independent S and C corrections are generated internally. Their amplitudes are adjustable by their respective I²C registers. They can also be inhibited by their select bits.

Finally, the amplitude of this S and C corrected ramp can be adjusted by the vertical ramp amplitude control register.

The adjusted ramp is available on Pin 23 (V_{OUT}) to drive an external power stage.

The gain of this stage can be adjusted (±25%) depending on its register value.

The mean value of this ramp is driven by its own I²C register (vertical position). Its value is VPOS = 7/16 · V_{REF-V} ± 300mV.

Usually VOUT is sent through a resistive divider to the inverting input of the booster. Since VPOS derives from V_{REF-V}, the bias voltage sent to the non-inverting input of the booster should also derive from V_{REF-V} to optimize the accuracy (see Application Diagram).

III.3 - Vertical Moiré

By using the vertical moiré, VPOS can be modulated from frame to frame. This function is intended to cancel the fringes which appear when line to line interval is very close to the CRT vertical pitch.

The amplitude of the modulation is controlled by register VMOIRE on sub-address 0C and can be switched-off via the control bit D7.

III.4 - Basic Equations

In first approximation, the amplitude of the ramp on Pin 23 (VOUT) is :

V_{OUT} - VPOS = (V_{OSC} - V_{DCMID}) · (1 + 0.25 (V_{AMP}))

with :

- V_{DCMID} = 7/16 · V_{REF} (middle value of the ramp on Pin 22, typically 3.5V)
- V_{OSC} = V_{22} (ramp with fixed amplitude)
- V_{AMP} = -1 for minimum vertical amplitude register value and +1 for maximum
- VPOS is calculated by : VPOS = V_{DCMID} + 0.3 V_P with V_P equals -1 for minimum vertical position register value and +1 for maximum

The current available on Pin 22 is :

$$I_{OSC} = \frac{3}{8} \cdot V_{REF} \cdot C_{OSC} \cdot f$$

with : C_{OSC} : capacitor connected on Pin 22 and
f : synchronization frequency.

III.5 - Geometric Corrections

The principle is represented in Figure 16.

Starting from the vertical ramp, a parabola-shaped current is generated for E/W correction (also known as Pin Cushion correction), dynamic horizontal phase control correction, and vertical dynamic Focus correction.

The parabola generator is made by an analog multiplier, the output current of which is equal to :

$$\Delta I = k \cdot (V_{OUT} - V_{DCMID})^2$$

where VOUT is the vertical output ramp (typically between 2 and 5V) and V_{DCMID} is 3.5V (for V_{REF-V} = 8V).

One more multiplier provides a current proportional to $(V_{OUT} - V_{DCMID})^4$ for corner correction.

The VOUT sawtooth is typically centered on 3.5V. By changing the vertical position, the sawtooth shifts by ±0.3V.

In order to have good screen geometry for any end user adjustment, the TDA9109/S has the "geometry tracking" feature, which allows generation of a dissymetric parabola depending on the vertical position.

Due to the large output stage voltage range (E/W, Keystone, Corner), the combination of tracking function with maximum vertical amplitude, maximum or minimum vertical position and maximum gain on the DAC control may lead to the output stage saturation. This must be avoided by limiting the output voltage with apropriate I²C registers values.

For the E/W part and the dynamic horizontal phase control part, a sawtooth-shaped differential current in the following form is generated :

$$\Delta I' = k' \cdot (V_{OUT} - V_{DCMID})$$

Then ΔI and ΔI' are added and converted into voltage for the E/W part.

Each of the three E/W components, and the two dynamic horizontal phase controls may be inhibited by their own I²C select bit.

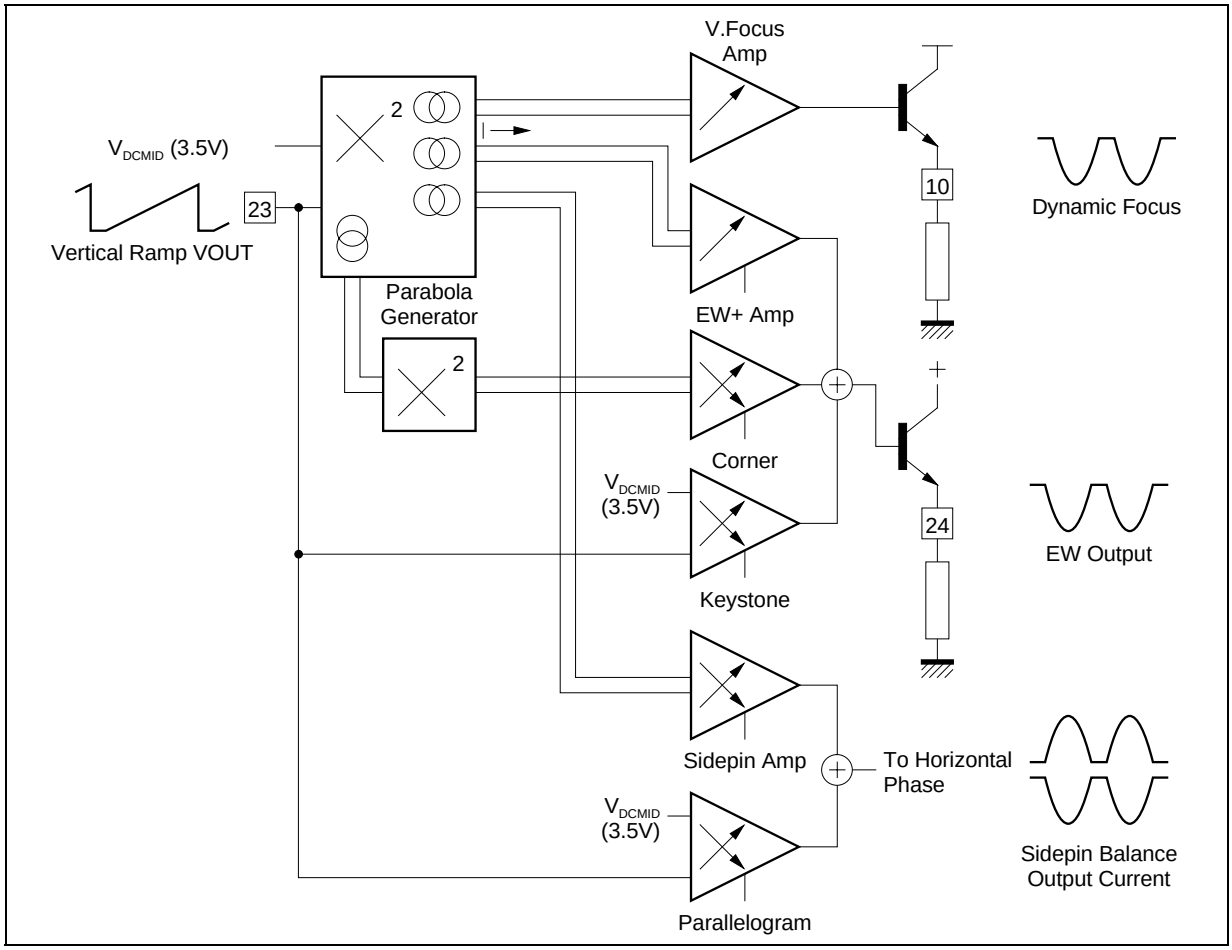
The E/W parabola is available on Pin 24 via an emitter follower output stage which has to be biased by an external resistor (10kΩ to ground). Since stable in temperature, the device can be DC coupled with an external circuitry.

The vertical dynamic focus is available on Pin 10.

The dynamic horizontal phase control drives internally the H-position, moving the HFLY position on the horizontal sawtooth in the range of ± 1.4% T_H both for side pin balance and parallelogram.

OPERATING DESCRIPTION (continued)

Figure 16 : Geometric Corrections Principle



III.6 - E/W

$EWOUT = 2.5V + K1 (V_{OUT} - V_{DCMID}) + K2 (V_{OUT} - V_{DCMID})^2 + K3 (V_{OUT} - V_{DCMID})^4$

K1 is adjustable by the keystone I^2C register,
K2 is adjustable by the E/W amplitude I^2C register,
K3 is adjustable by the corner I^2C register.

III.7 - Dynamic Horizontal Phase Control

$I_{OUT} = K4 (V_{OUT} - V_{DCMID}) + K5 (V_{OUT} - V_{DCMID})^2$

K4 is adjustable by the parallelogram I^2C register,
K5 is adjustable by the side pin balance I^2C register.

OPERATING DESCRIPTION (continued)

IV - DC/DC CONVERTER PART

This unit controls the switch-mode DC/DC converter. It converts a DC constant voltage into the B+ voltage (roughly proportional to the horizontal frequency) necessary for the horizontal scanning. ThisDC/DC converter must be configured in step-up mode. It operates very similarly to the well known UC3842.

IV.1 - Step-up Mode
Operating Description

- The power MOS is switched-on at the middle of the horizontal flyback.
- The power MOS is switched-off when its current reaches a predetermined value. For this purpose, a sense resistor is inserted in its source. The voltage on this resistor is sent to Pin16 (I_{SENSE}).
- The feedback (coming either from the EHV or from the flyback) is divided to a voltage close to 4.8V and compared to the internal 4.8V reference (I_{VREF}). The difference is amplified by an error amplifier, the output of which controls the power MOS switch-off current.

Main Features

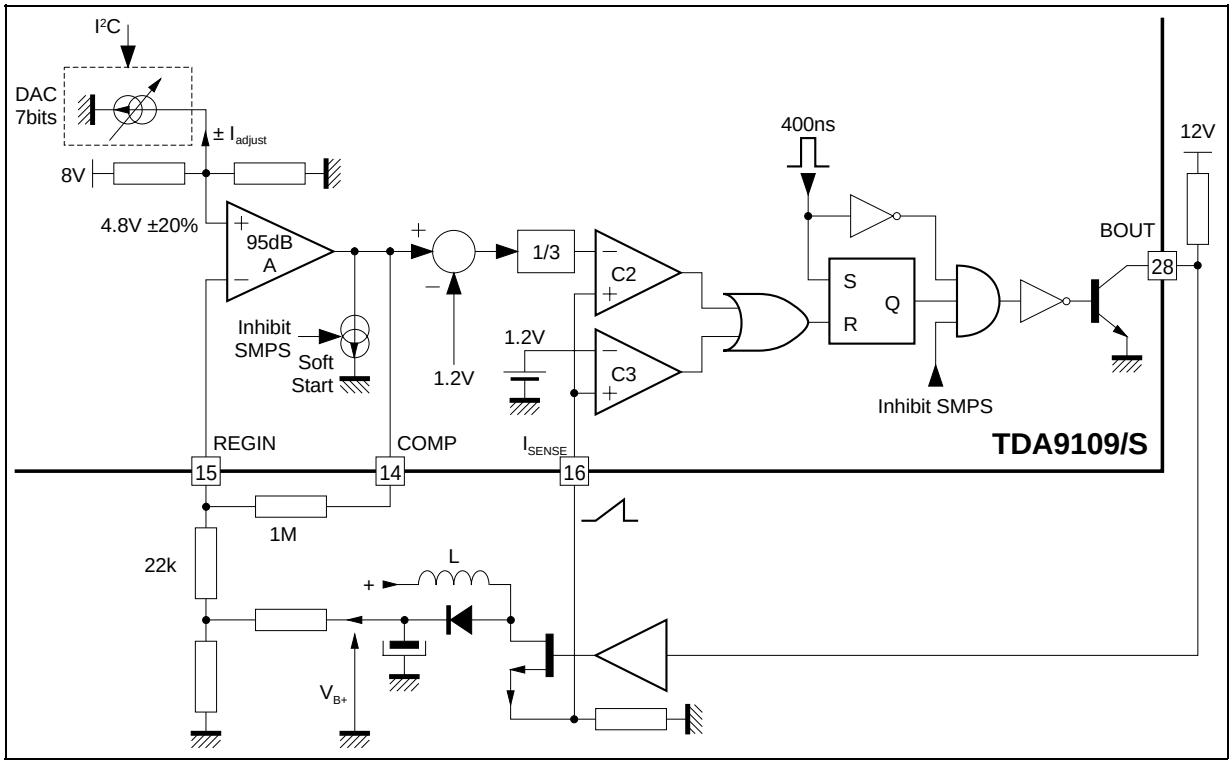
- Switching synchronized on the horizontal frequency,
- B+ voltage always higher than the DC source,
- Current limited on a pulse-by-pulse basis.

The DC/DC converter is disabled :

- when V_{CC} or V_{DD} are too low,
- when X-Ray protection is latched,
- directly through I^2C bus.

When disabled, BOUT is driven to GND by a 0.5mA current source. This feature allows to implement externally a soft start circuit.

Figure 17 : DC/DC Converter



INTERNAL SCHEMATICS

Figure 18

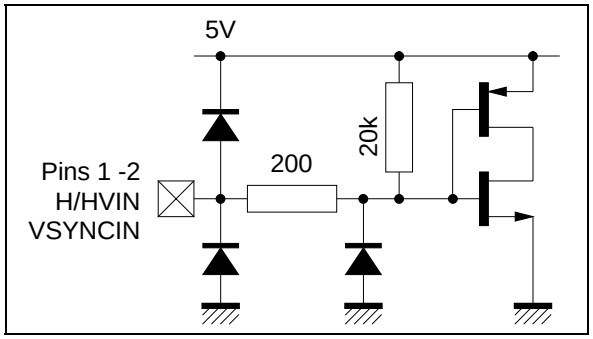


Figure 19

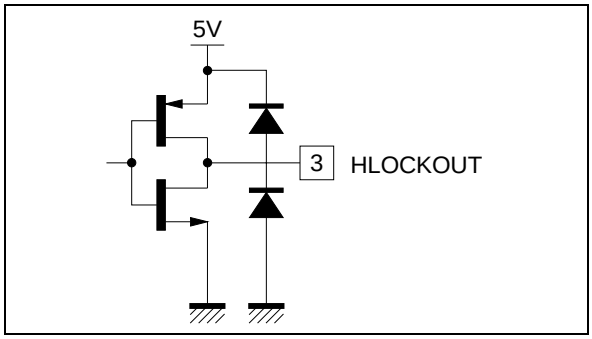


Figure 20

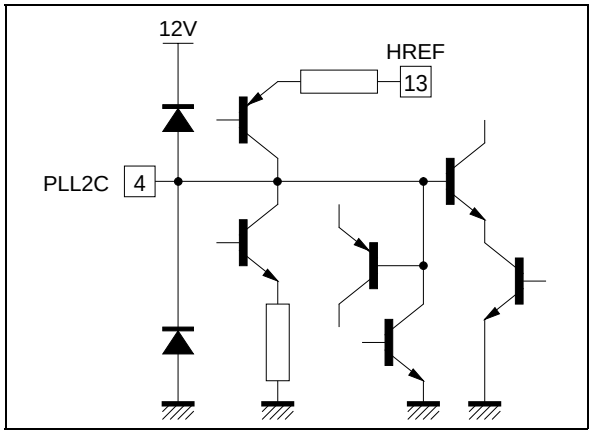


Figure 21

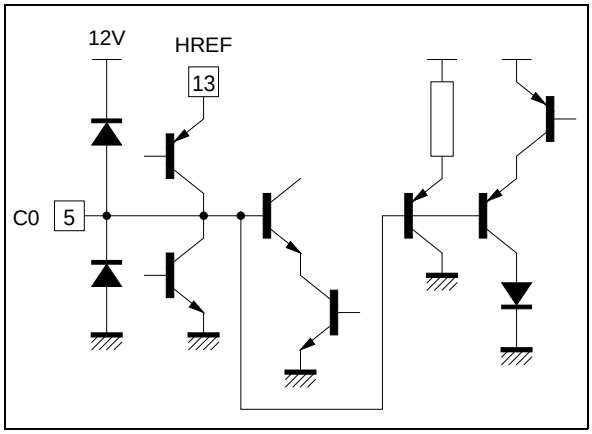


Figure 22

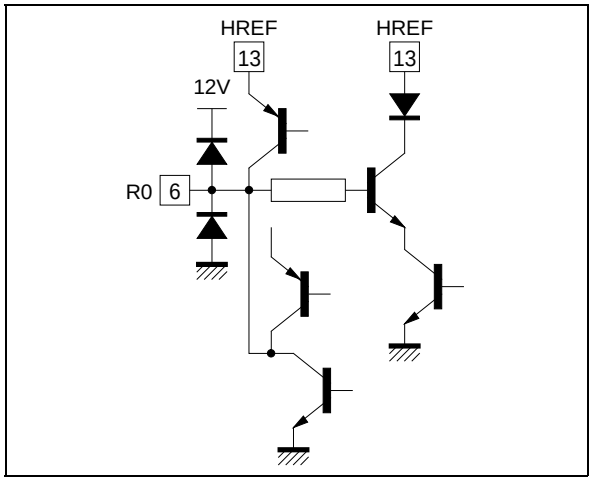
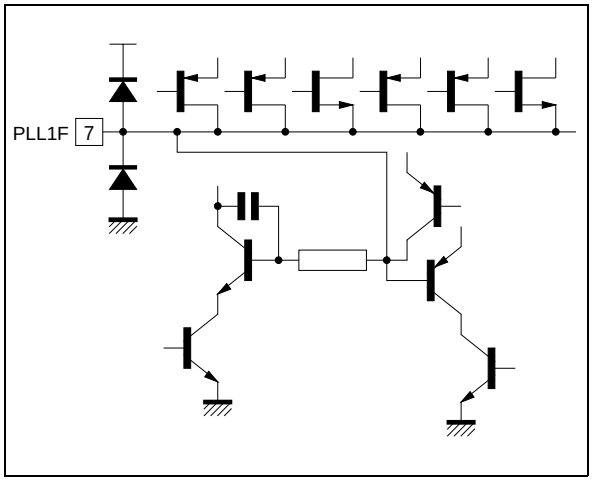


Figure 23



INTERNAL SCHEMATICS (continued)

Figure 24

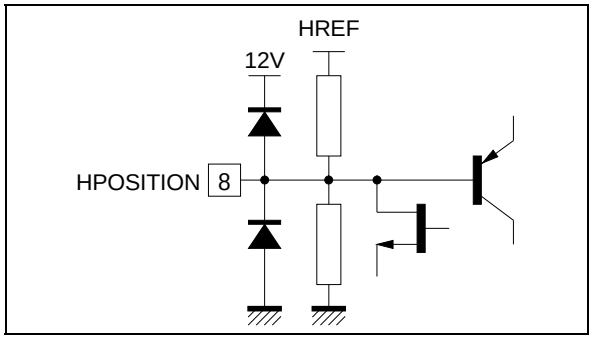


Figure 25

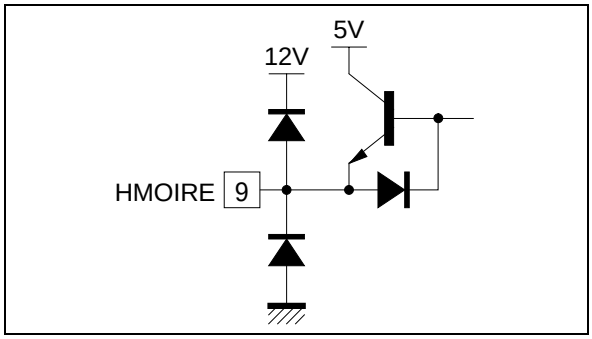


Figure 26

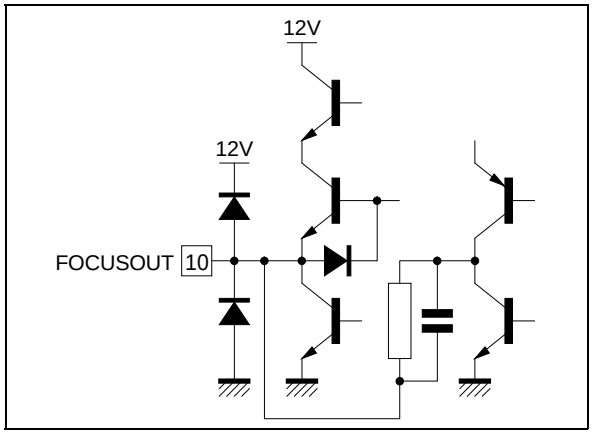


Figure 27

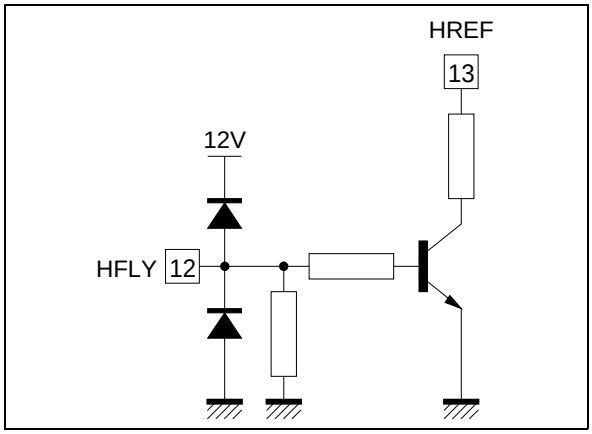


Figure 28

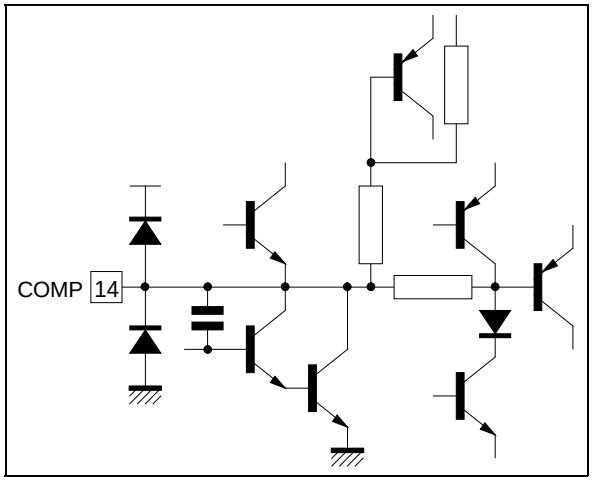
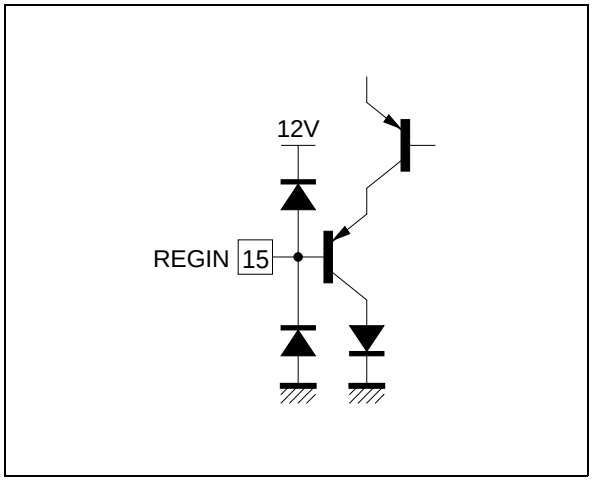


Figure 29



INTERNAL SCHEMATICS (continued)

Figure 30

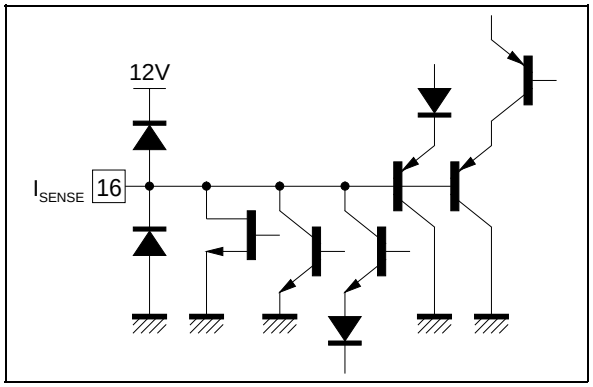


Figure 31

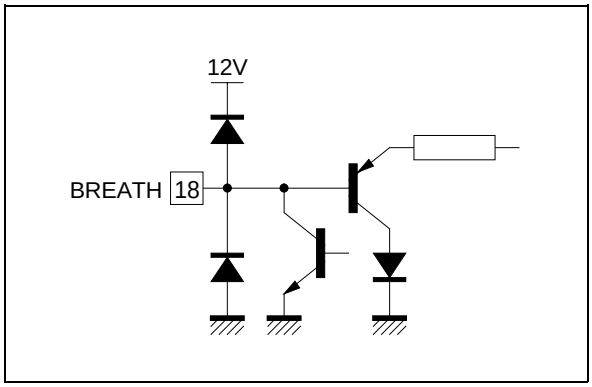


Figure 32

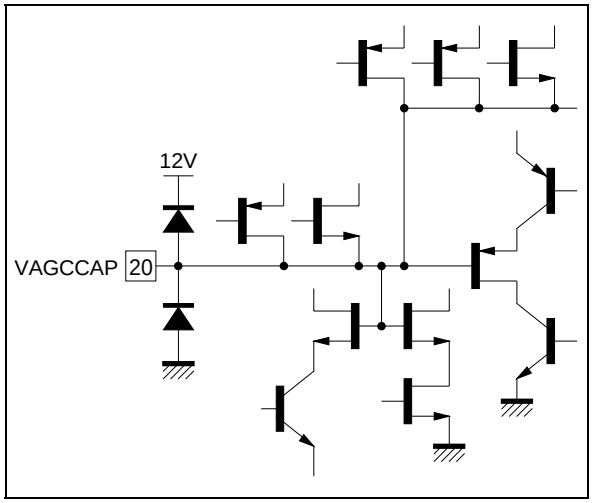


Figure 33

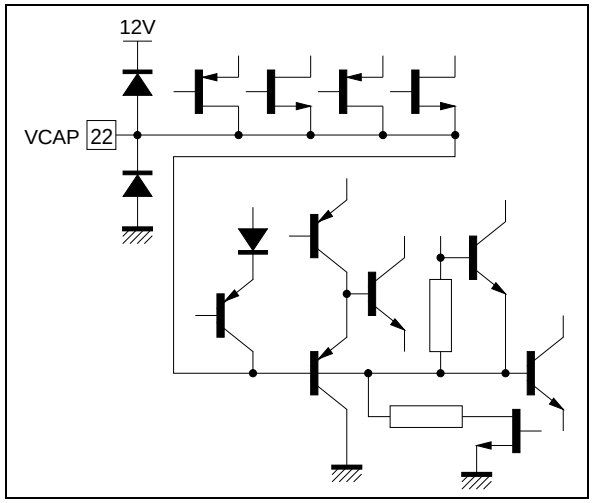


Figure 34

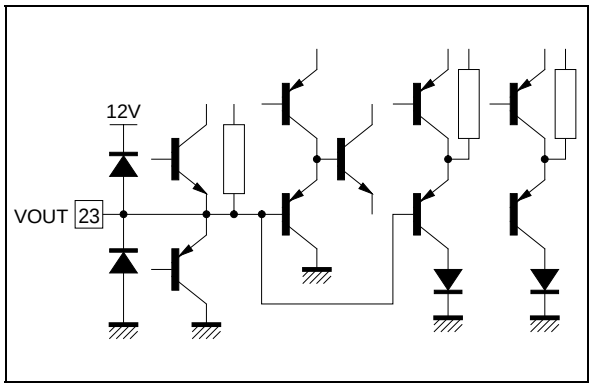
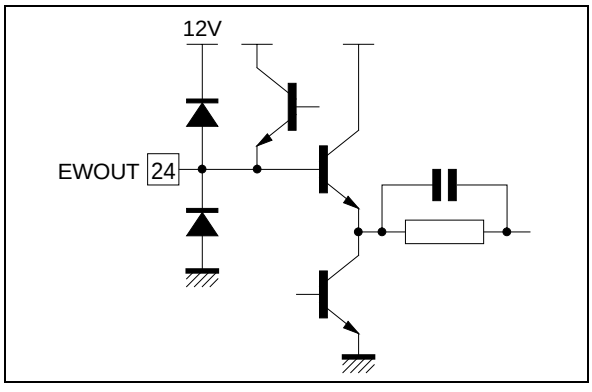


Figure 35



INTERNAL SCHEMATICS (continued)

Figure 36

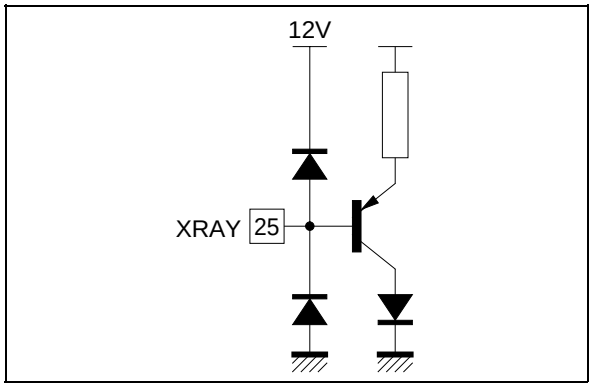


Figure 37

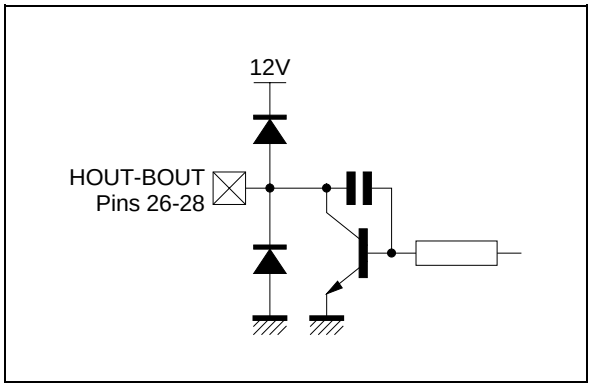
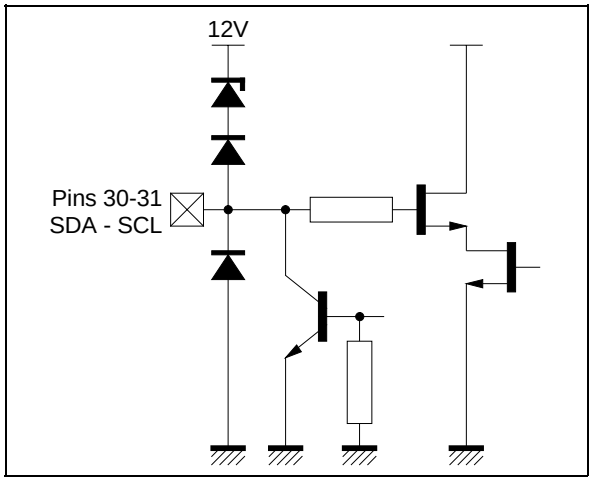
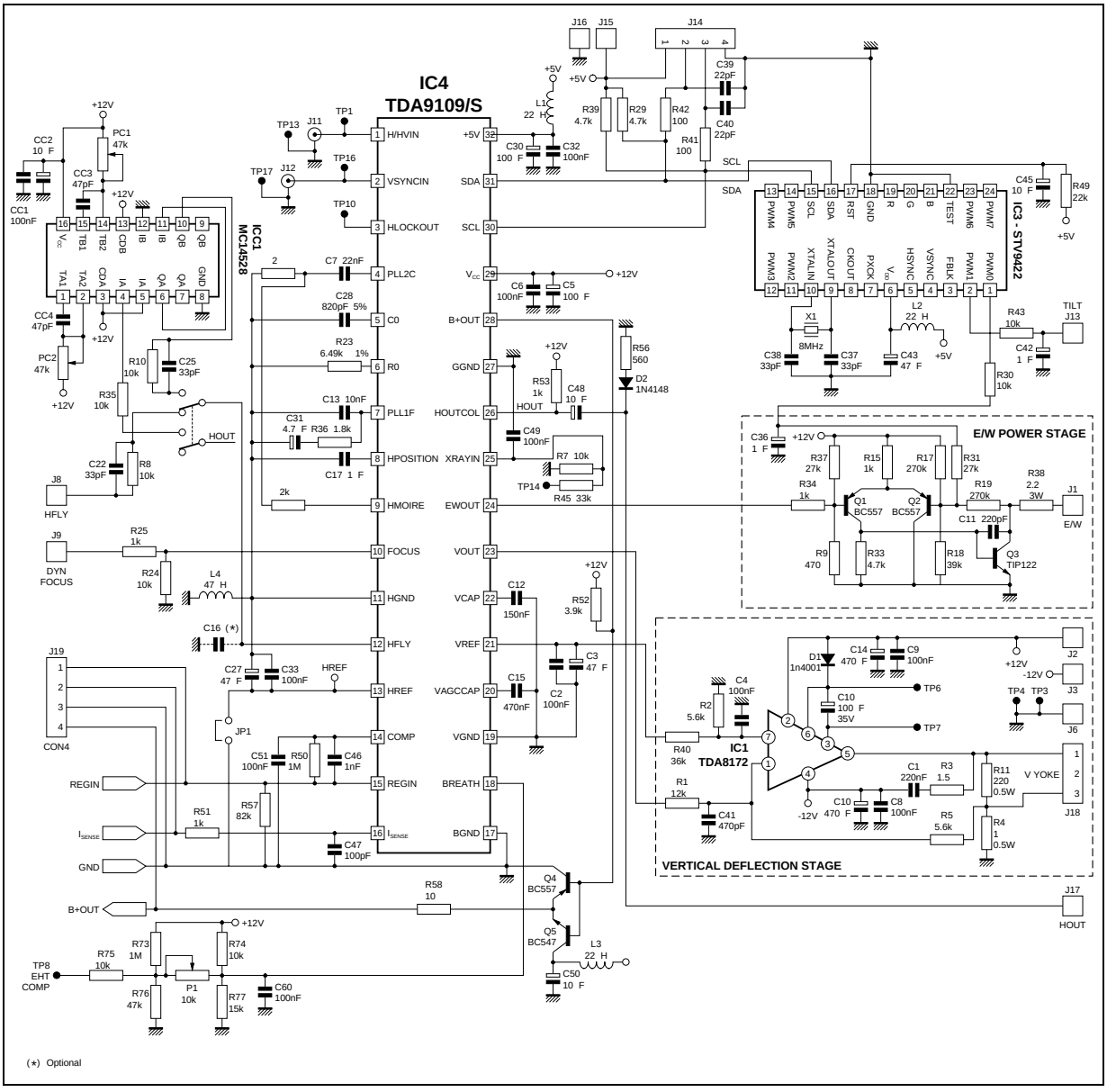


Figure 38



APPLICATION DIAGRAMS

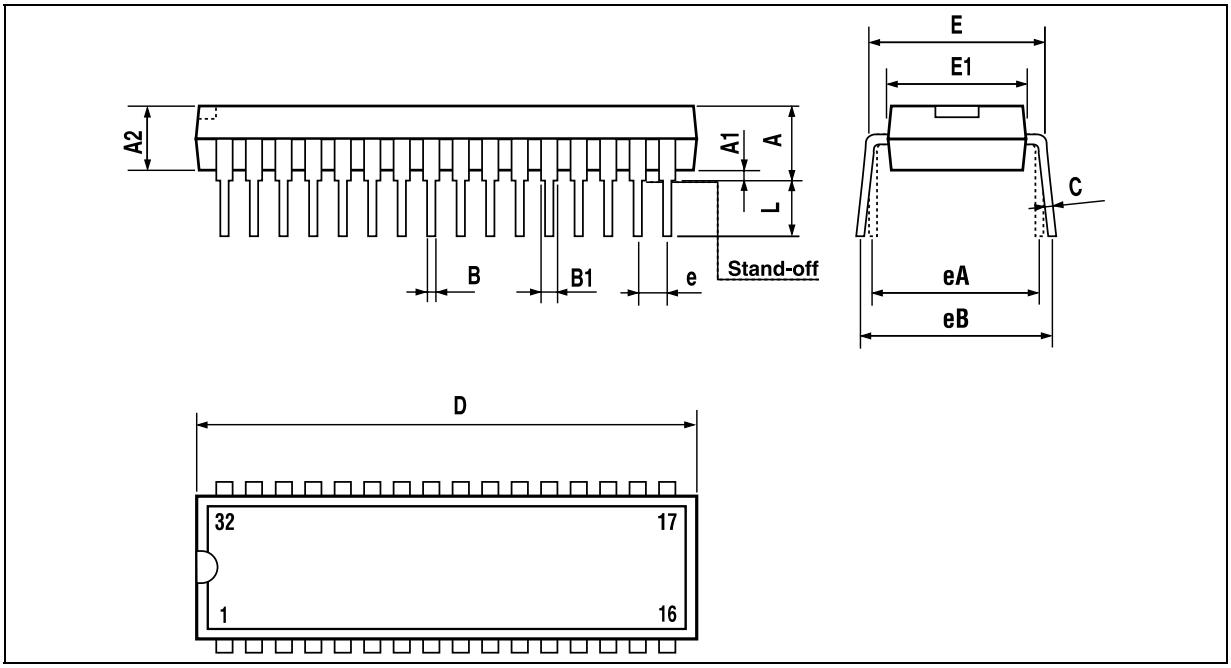
Figure 39 : Demonstration Board



The difference with standard TDA9109 Application Diagram is the resistor divider 2kΩ/2Ω on Pin 9 (HMOIRE).

PACKAGE MECHANICAL DATA

32 PINS - PLASTIC SHRINK DIP



PMSDIP32.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	3.556	3.759	5.080	0.140	0.148	0.200
A1	0.508			0.020		
A2	3.048	3.556	4.572	0.120	0.140	0.180
B	0.356	0.457	0.584	0.014	0.018	0.023
B1	0.762	1.016	1.397	0.030	0.040	0.055
C	0.203	0.254	0.356	0.008	0.010	0.014
D	27.43	27.94	28.45	1.080	1.100	1.120
E	9.906	10.41	11.05	0.390	0.410	0.435
E1	7.620	8.890	9.398	0.300	0.350	0.370
e		1.778			0.070	
eA		10.16			0.400	
eB			12.70			0.500
L	2.540	3.048	3.810	0.100	0.120	0.150

SDIP32.TBL