DATA SHEET

TSA5512
1.3 GHz Bidirectional I^2C-bus controlled synthesizer

Product specification
File under Integrated Circuits, IC02

October 1992

Philips
Semiconductors

PHILIPS

1.3 GHz Bidirectional I²C-bus controlled synthesizer TSA5512

FEATURES

- Complete 1.3 GHz single chip system
- Low power 5 V, 35 mA
- I²C-bus programming
- In-lock flag
- Varicap drive disable
- Low radiation
- Address selection for Picture-In-Picture (PIP), DBS tuner (3 addresses)
- Analog-to-digital converter
- 8 bus controlled ports (6 for TSA5512T), 8 open collector outputs (4 bidirectional)
- Power-down flag

APPLICATIONS

- TV tuners
- VCR Tuners

DESCRIPTION

The TSA5512 is a single chip PLL frequency synthesizer designed for TV tuning systems. Control data is entered via the I²C-bus; five serial bytes are required to address the device, select the oscillator frequency, programme the eight output ports and set the charge-pump current. Four of these ports can also be used as input ports (three general purpose I/O ports, one ADC). Digital information concerning those ports can be read out of the TSA5512 on the SDA line (one status byte) during a READ operation. A flag is set when the loop is “in-lock” and is read during a READ operation. The device has one fixed I²C-bus address and 3 programmable addresses, programmed by applying a specific voltage on Port 3. The phase comparator operates at 7.8125 kHz when a 4 MHz crystal is used.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TSA5512	18	DIL	plastic	SOT102(1)
TSA5512T	16	SO	plastic	SOT109A(2)
TSA5512AT	20	SO	plastic	SOT163A(3)
TSA5512M	20	SSOP	plastic	SOT266(4)

Note

1. SOT102-1; 1996 December 5.
2. SOT109-1; 1996 December 5.
3. SOT163-1; 1996 December 5.
4. SOT266-1; 1996 December 5.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	–	5	–	V
I_{CC}	supply current	–	35	–	mA
Δfr	frequency range	64	–	1300	MHz
V_I	input voltage level				
	80 MHz to 150 MHz	12	–	300	mV
	150 MHz to 1 GHz	9	–	300	mV
	1 GHz to 1.3 GHz	40	–	300	mV
f_{XTAL}	crystal oscillator frequency	3.2	4.0	4.48	MHz
I_O	open-collector output current	5	–	–	mA
T_{amb}	operating ambient temperature range	–10	–	+80	°C
T_{stg}	IC storage temperature range	–40	–	+150	°C

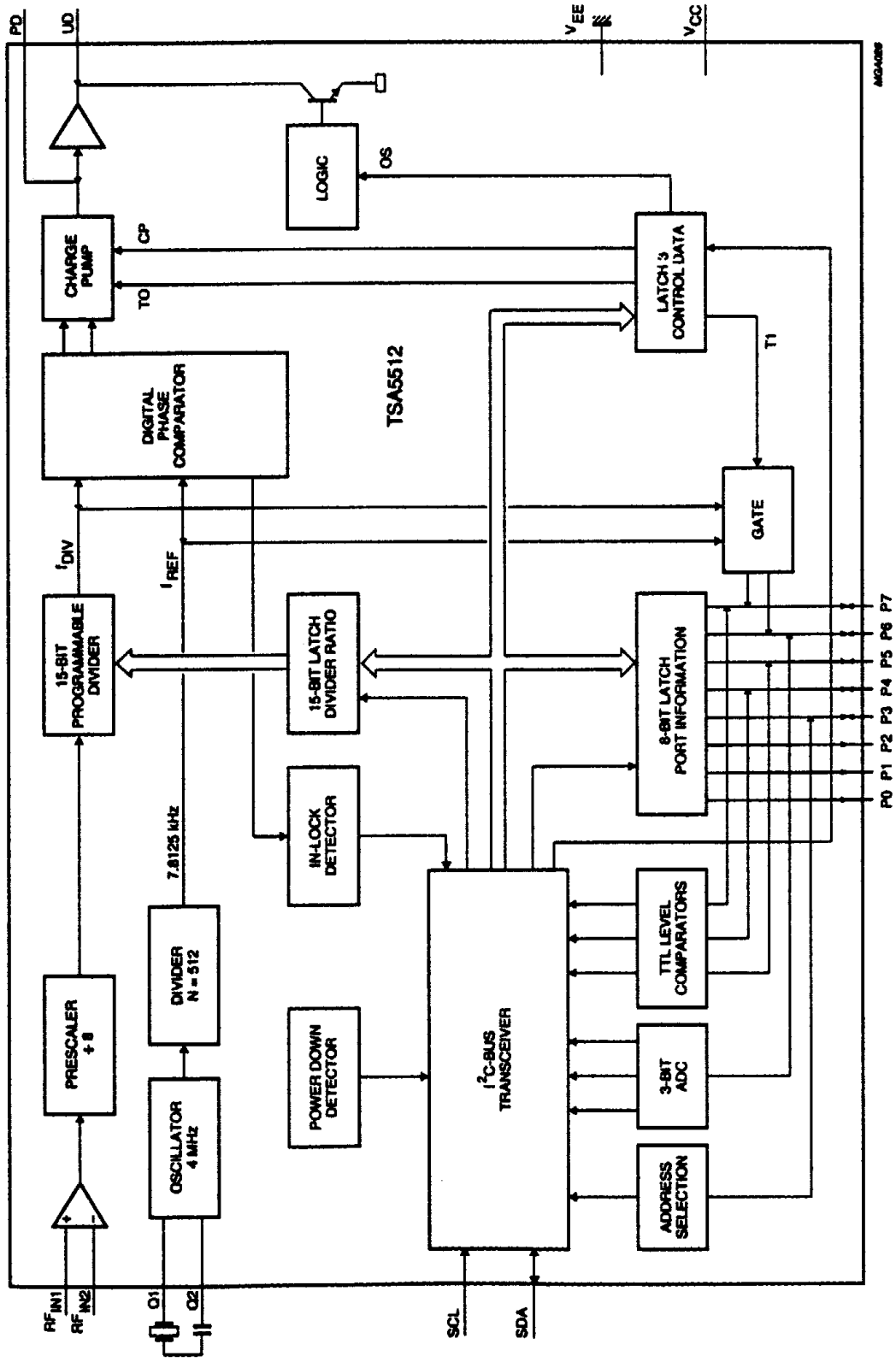


Fig.1 Block diagram.

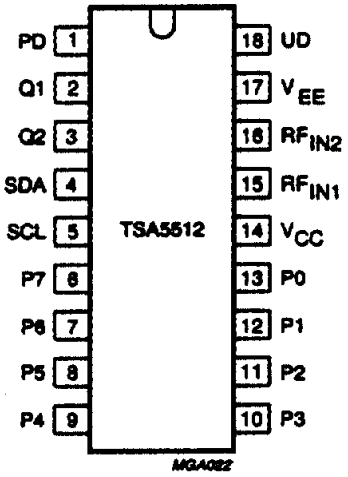


Fig.2 Pin configuration for SOT102.

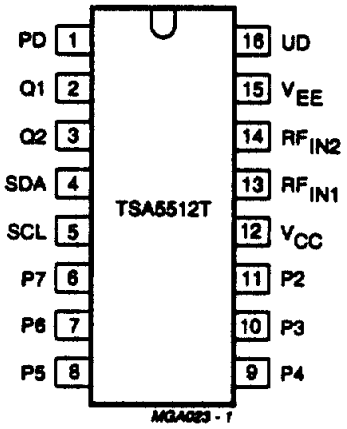


Fig.3 Pin configuration for SOT109.

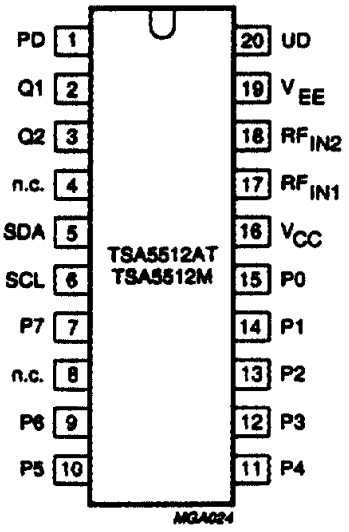


Fig.4 Pin configuration for SOT163/SOT266.

PINNING

SYMBOL	PIN			DESCRIPTION
	SOT102	SOT109	SOT163 SOT266	
PD	1	1	1	charge-pump output
Q1	2	2	2	crystal oscillator input 1
Q2	3	3	3	crystal oscillator reference voltage
n.c.	–	–	4	not connected
SDA	4	4	5	serial data input/output
SCL	5	5	6	serial clock input
P7	6	6	7	port output/input (general purpose)
n.c.	–	–	8	not connected
P6	7	7	9	port output/input for general purpose ADC
P5	8	8	10	port output/input (general purpose)
P4	9	9	11	port output/input (general purpose)
P3	10	10	12	port output/input for address selection
P2	11	11	13	port output
P1	12	–	14	port output
P0	13	–	15	port output
V_{CC}	14	12	16	voltage supply
RF_{IN1}	15	13	17	UHF/VHF signal input 1
RF_{IN2}	16	14	18	UHF/VHF signal input 2 (decoupled)
V_{EE}	17	15	19	ground
UD	18	16	20	drive output

FUNCTIONAL DESCRIPTION

The TSA5512 is controlled via the two-wire I²C-bus. For programming, there is one module address (7 bits) and the R/$\overline{W}$ bit for selecting READ or WRITE mode.

WRITE mode: R/$\overline{W}$ = 0 (see Table 1)

After the address transmission (first byte), data bytes can be sent to the device. Four data bytes are required to fully program the TSA5512. The bus transceiver has an auto-increment facility which permits the programming of the TSA5512 within one single transmission (address + 4 data bytes).

The TSA5512 can also be partially programmed on the condition that the first data byte following the address is byte 2 or byte 4. The meaning of the bits in the data bytes is given in Table 1. The first bit of the first data byte transmitted indicates whether frequency data (first bit = 0) or charge pump and port information (first bit = 1) will follow. Until an I²C-bus STOP condition is sent by the controller, additional data bytes can be entered without the need to re-address the device. This allows a smooth frequency sweep for fine tuning or AFC purpose. At power-on the ports are set to the high impedance state.

The 7.8125 kHz reference frequency is obtained by dividing the output of the 4 MHz crystal oscillator by 512. Because the input of UHF/VHF signal is first divided by 8 the step size is 62.5 kHz. A 3.2 MHz crystal can offer step sizes of 50 kHz.

Table 1 Write data format

	MSB							**LSB**		
Address	1	1	0	0	0	MA1	MA0	0	A	byte 1
Programmable divider	0	N14	N13	N12	N11	N10	N9	N8	A	byte 2
Programmable divider	N7	N6	N5	N4	N3	N2	N1	N0	A	byte 3
Charge-pump and test bits	1	CP	T1	T0	1	1	1	OS	A	byte 4
Output ports control bits	P7	P6	P5	P4	P3	P2	P1*	P0*	A	byte 5

Note to Table 1

*	not valid for TSA5512T
MA1,MAO	programmable address bits (see Table 4)
A	acknowledge bit
N14 to N0	programmable divider bits
$N = N14 \times 2^{14} + N13 \times 2^{13} + ... + N1 \times 2^{1} + NO$	
CP	charge-pump current
CP = 0	50 μA
CP = 1	220 μA
P7 to P0 = 1	open-collector output is active
P7 to P0 = 0	outputs are in high impedance state
T1, T0, OS = 0 0 0	normal operation
T1 = 1	$P6 = f_{ref}$, $P7 = f_{DIV}$
T0 = 1	3-state charge-pump
OS = 1	operational amplifier output is switched off (varicap drive disable)

READ mode: R/$\overline{W}$ = 1 (see Table 2)

Data can be read out of the TSA5512 by setting the R/$\overline{W}$ bit to 1. After the slave address has been recognized, the TSA5512 generates an acknowledge pulse and the first data byte (status word) is transferred on the SDA line (MSB first). Data is valid on the SDA line during a high position of the SCL clock signal. A second data byte can be read out of the TSA5512 if the processor generates an acknowledge on the SDA line. End of transmission will occur if no acknowledge from the processor occurs. The TSA5512 will then release the data line to allow the processor to generate a STOP condition. When ports P3 to P7 are used as inputs, they must be programmed in their high-impedance state. The POR flag (power-on reset) is set to 1 when V_{CC} goes below 3 V and at power-on. It is reset when an end of data is detected by the TSA5512 (end of a READ sequence). Control of the loop is made possible with the in-lock flag FL which indicates (FL = 1) when the loop is phase-locked. The bits I2, I1 and I0 represent the status of the I/O ports P7, P5 and P4 respectively. A logic 0 indicates a LOW level and a logic 1 a HIGH level (TTL levels). A built-in 5-level ADC is available on I/O port P6. This converter can be used to feed AFC information to the controller from the IF section of the television as illustrated in the typical application circuit (Fig.8). The relationship between bits A2, A1 and A0 and the input voltage on port P6 is given in Table 3.

Table 2 Read data format

	MSB							**LSB**		
Address	1	1	0	0	0	MA1	MA0	1	A	byte 1
Status byte	POR	FL	I2	I1	I0	A2	A1	A0	–	byte 2

Note to Table 2

POR	power-on reset flag. (POR = 1 on power-on)
FL	in-lock flag (FL = 1 when the loop is phase-locked)
I2, I1, I0	digital information for I/O ports P7, P5 and P4 respectively
A2, A1 A0	digital outputs of the 5-level ADC. Accuracy is 1/2 LSB (see Table 3)

MSB is transmitted first

Address selection

The module address contains programmable address bits (MA1 and MA0) which together with the I/O port P3 offers the possibility of having several synthesizers (up to 3) in one system.
The relationship between MA1 and MA0 and the input voltage I/O port P3 is given in Table 4

Table 3 ADC levels

VOLTAGE APPLIED ON THE PORT P6	A2	A1	A0
0.6 V_{CC} to 13.5 V	1	0	0
0.45 V_{CC} to 0.6 V_{CC}	0	1	1
0.3 V_{CC} to 0.45 V_{CC}	0	1	0
0.15 V_{CC} to 0.3 V_{CC}	0	0	1
0 to 0.15 V_{CC}	0	0	0

Table 4 Address selection

MA1	MA0	VOLTAGE APPLIED ON PORT P3
0	0	0 to 0.1 V_{CC}
0	1	always valid
1	0	0.4 to 0.6 V_{CC}
1	1	0.9 V_{CC} to 13.5 V

LIMITING VALUES

In accordance with Absolute Maximum Rating System (IEC 134); all pin numbers refer to DIL18 version

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–0.3	6	V
V_1	charge-pump output voltage	–0.3	V_{CC}	V
V_2	crystal (Q1) input voltage	–0.3	V_{CC}	V
V_4	serial data input/output voltage	–0.3	6	V
V_5	serial clock input voltage	–0.3	6	V
$V_{6\text{-}13}$	P7 to P0 input/output voltage	–0.3	+16	V
V_{15}	prescaler input voltage	–0.3	V_{CC}	V
V_{18}	drive output voltage	–0.3	V_{CC}	V
$I_{6\text{-}13}$	P7 to P0 output current (open collector)	–1	15	mA
I_4	SDA output current (open collector)	–1	5	mA
T_{stg}	IC storage temperature range	–40	+150	°C
T_j	maximum junction temperature	–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	DIL18	80 K/W
	SO16	110 K/W
	SO20	80 K/W
	SSOP20	120 K/W

CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = 25 °C, unless otherwise specified

All pin numbers refer to DIL18 version

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Functional range						
V_{CC}	supply voltage range		4.5	–	5.5	V
T_{amb}	operating ambient temperature range		–10	–	+80	°C
f	input frequency		64	–	1300	MHz
N	divider		256	–	32767	
I_{CC}	supply current		25	35	50	mA
f_{XTAL}	crystal oscillator frequency range	crystal series resonance resistance ≤ 150 Ω	3.2	4.0	4.48	MHz
Z_I	input impedance (pin 2)		–480	–400	–320	Ω
	input level	V_{CC} = 4.5 V to 5.5 V; T_{amb} = –10 to +80 °C; see typical sensitivity curve Fig.6				
	f = 80 to 150 MHz		12/–25	–	300/2.6	mV/dBm
	f = 150 to 1000 MHz		9/–28	–	300/2.6	mV/dBm
	f = 1000 to 1300 MHz		40/–15	–	300/2.6	mV/dBm
R_I	prescaler input resistance (see Fig.7)		–	50	–	Ω
C_I	input capacitance		–	2	–	pF
Output ports (open collector) P0 to P7 (see note 1)						
I_{LO}	output leakage current	V_O = 13.5 V	–	–	10	µA
V_{OL}	LOW level output voltage	I_{OL} = 5 mA; note 2	–	–	0.7	V
Input port P3						
I_{OH}	HIGH level input current	V_{OH} = 13.5 V	–	–	10	µA
I_{OL}	LOW level input current	V_{OL} = 0 V	–10	–	–	µA
Input ports P4, P5 and P7						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		2.7	–	–	V
I_{IH}	HIGH level input current	V_{IH} = 13.5 V	–	–	10	µA
I_{IL}	LOW level input current	V_{IL} = 0 V	–10	–	–	µA
Input port P6						
I_{IH}	HIGH level input current	V_{IH} = 13.5 V	–	–	10	µA
I_{IL}	LOW level input current	V_{IL} = 0 V	–10	–	–	µA
SCL and SDA inputs						
V_{IH}	HIGH level input voltage		3.0	–	5.5	V
V_{IL}	LOW level input voltage		–	–	1.5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SCL and SDA inputs						
I_{IH}	HIGH level input current	V_{IH} = 5 V; V_{CC} = 0 V	–	–	10	µA
		V_{IH} = 5 V; V_{CC} = 5 V	–	–	10	µA
I_{IL}	LOW level input current	V_{IL} = 0 V; V_{CC} = 0 V	–10	–	–	µA
		V_{IL} = 0 V; V_{CC} = 5 V	–10	–	–	µA
Output SDA (pin 4; open collector)						
I_{LO}	output leakage current	V_O = 5.5 V	–	–	10	µA
V_O	output voltage	I_O = 3 mA	–	–	0.4	V
Charge-pump output PD (pin 1)						
I_{OH}	HIGH level output current (absolute value)	CP = 1	90	220	300	µA
I_{OL}	LOW level output current (absolute value)	CP = 0	22	50	75	µA
V_1	output voltage	in-lock	1.5	–	2.5	V
I_{1leak}	off-state leakage current	T0 = 1	–5	–	5	nA
Operational amplifier output UD (test mode T0 = 1)						
V_{18}	output voltage	V_{IL} = 0 V	–	–	100	mV
V_{18}	output voltage when switched-off	OS = 1; V_{IL} = 2 V	–	–	200	mV
G	operational amplifier current gain; $I_{18}/(I_1 - I_{1leak})$	OS = 0; V_{IL} = 2 V; I_{18} = 10 µA	2000	–	–	

Notes to the characteristics

1. When a port is active, the collector voltage must not exceed 6 V.
2. Measured with all open-collector ports active.

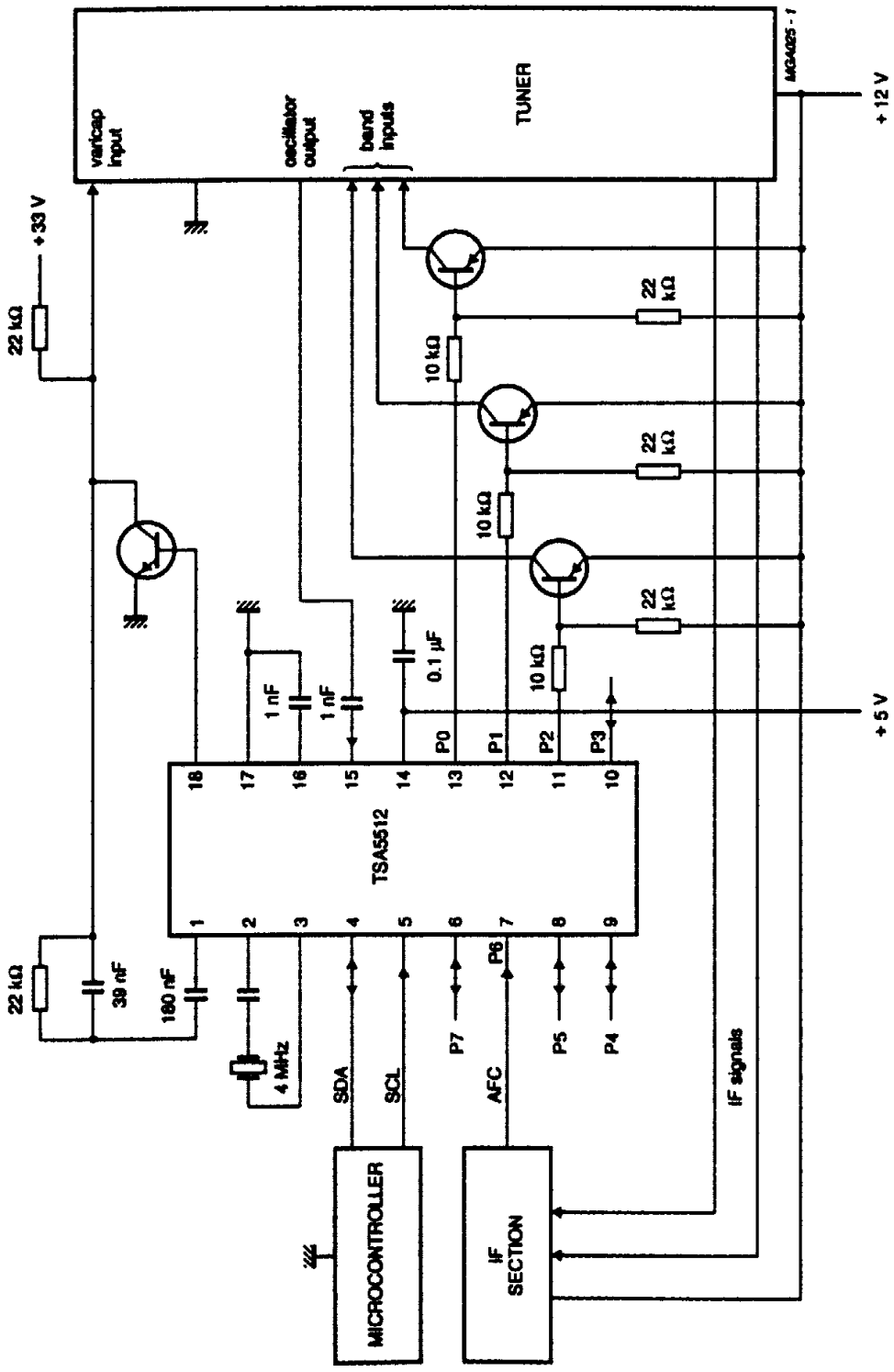


Fig.5 Typical application (DIL18).

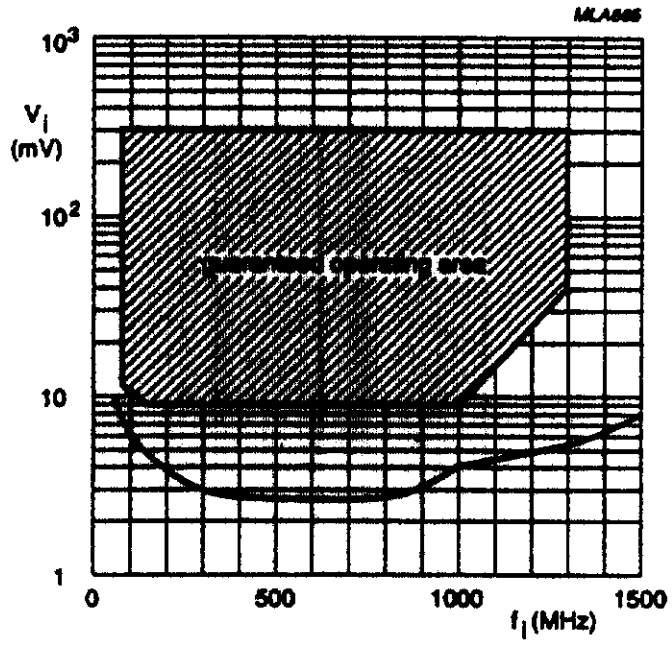


Fig.6 Prescaler typical input sensitivity curve; V_{CC} = 4.5 to 5.5 V; T_{amb} = –10 to +80 °C.

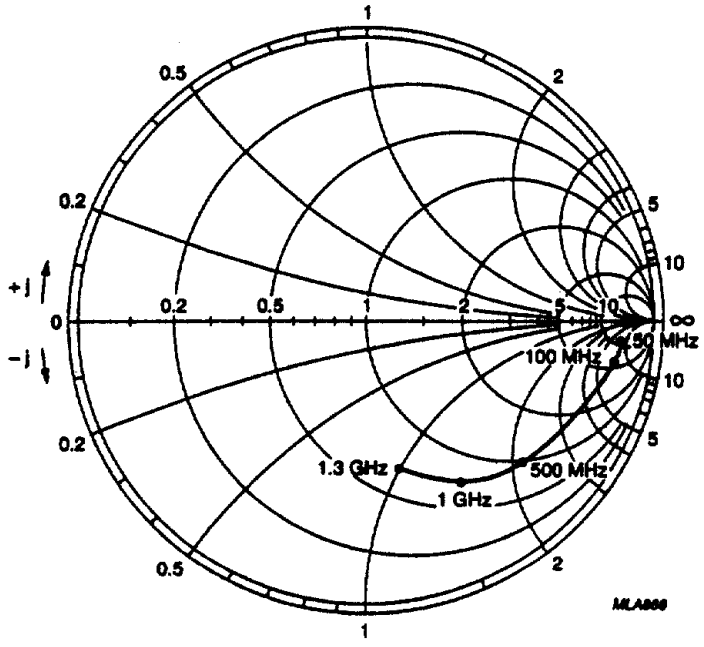


Fig.7 Prescaler Smith chart of typical input impedance; V_{CC} = 5 V; reference value = 50 Ω.

FLOCK FLAG DEFINITION (FL)

When the FL flag is 1, the maximum frequency deviation (Δf) from stable frequency can be expressed as follows:

$\Delta f = \pm (K_{VCO}/K_O) \times I_{CP} \times (C1 + C2)/(C1 \times C2)$

Where:

K_{VCO}	=	oscillator slope (Hz/V)
I_{CP}	=	charge-pump current (A)
K_O	=	$4 \times 10E6$
C1 and C2	=	loop filter capacitors (see Fig.8)

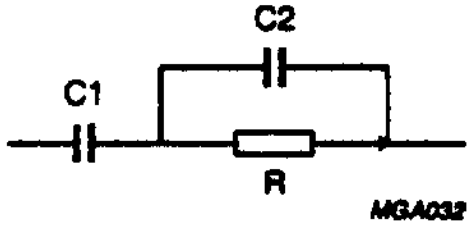


Fig.8 Loop filter.

FLOCK FLAG APPLICATION

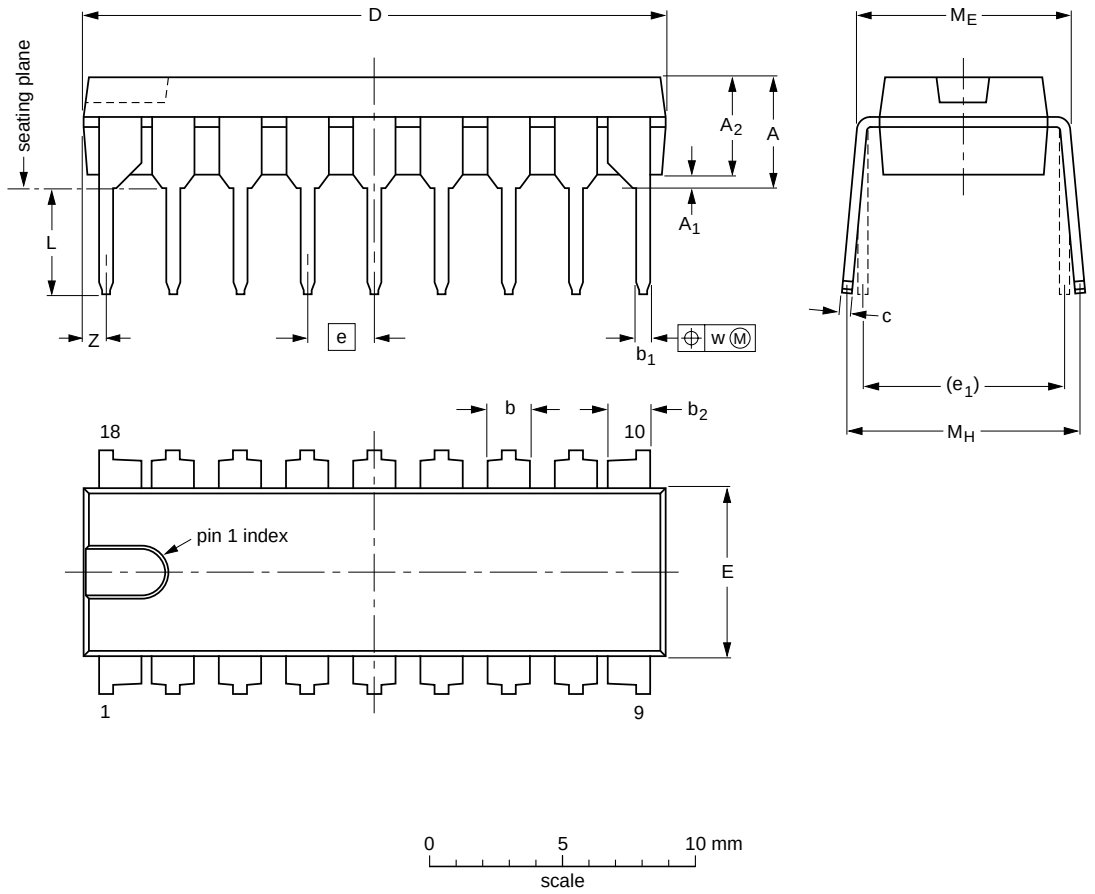
- K_{VCO} = 16 MHz/V (UHF band)
- I_{CP} = 220 mA
- C1 = 180 nF
- C2 = 39 nF
- Δf = ± 27.5 kHz.

Table 5 Flock flag settings

	MIN.	MAX.	UNIT
Time span between actual phase lock and FL-flag setting	1024	1152	µs
Time span between the loop losing lock and FL-flag resetting	0	128	µs

PACKAGE OUTLINE

DIP18: plastic dual in-line package; 18 leads (300 mil) **SOT102-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

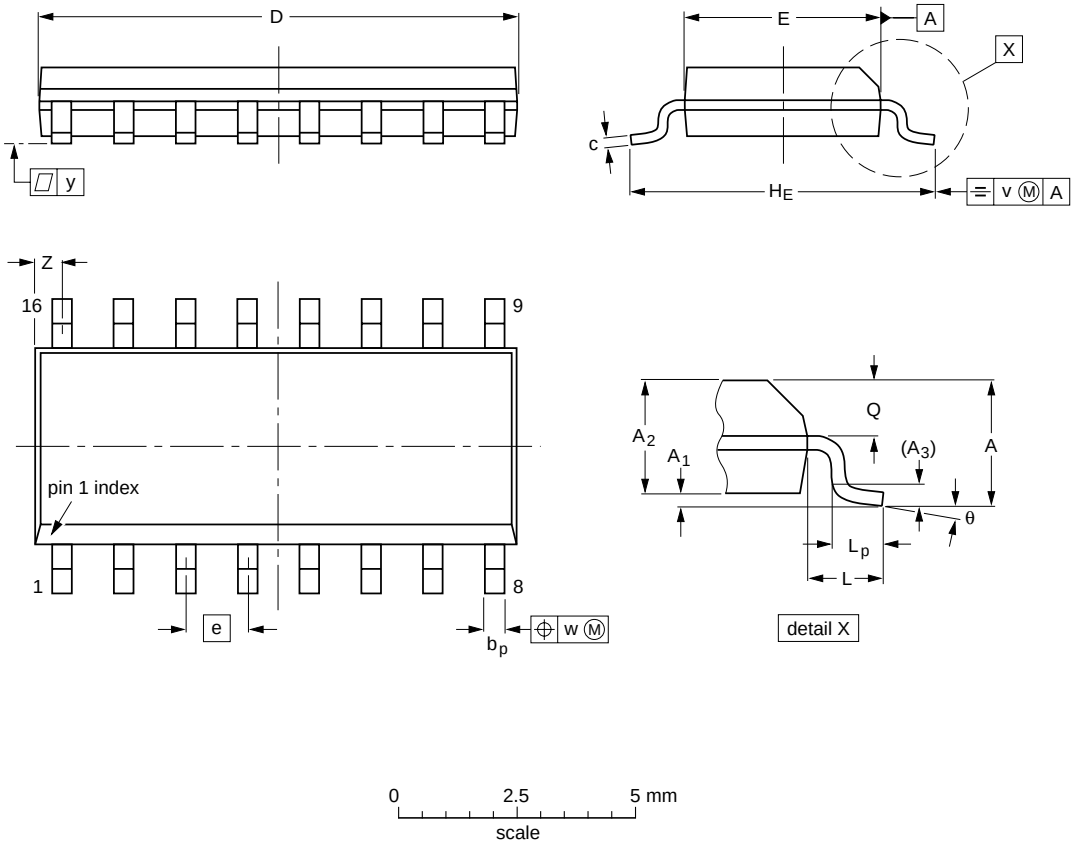
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	1.40 1.14	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	0.85
inches	0.19	0.020	0.15	0.055 0.044	0.021 0.015	0.055 0.044	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.033

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT102-1						~~93-10-14~~ 95-01-23

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

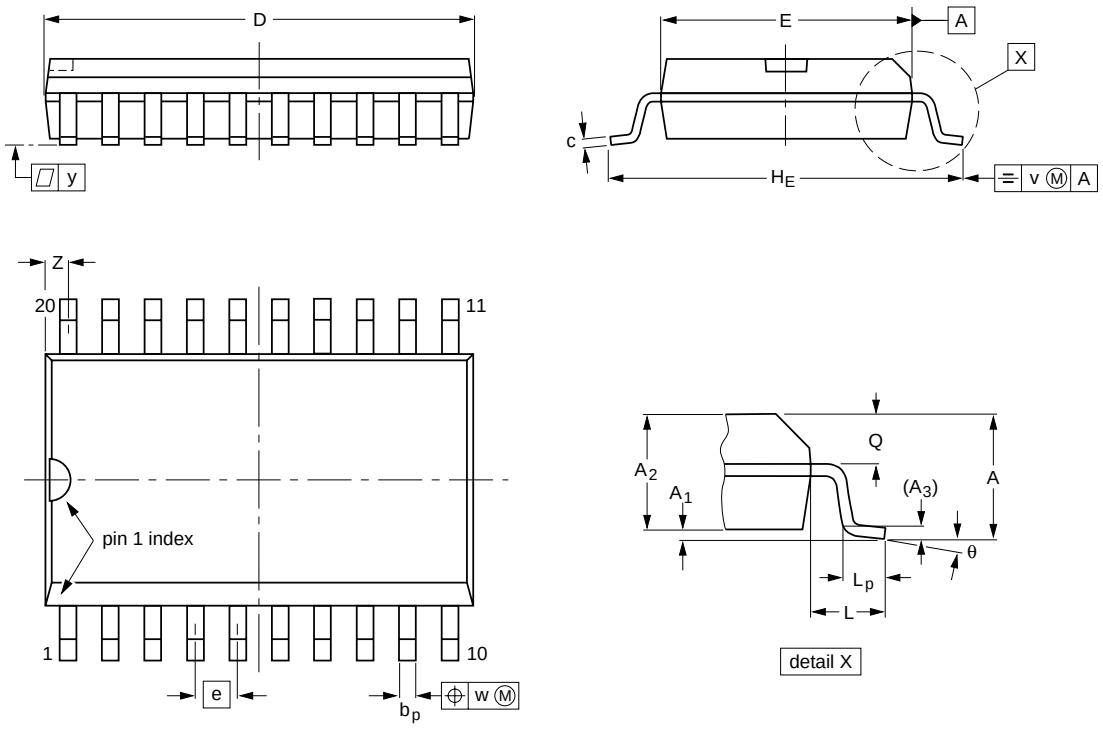
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~95-01-23~~ 97-05-22

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

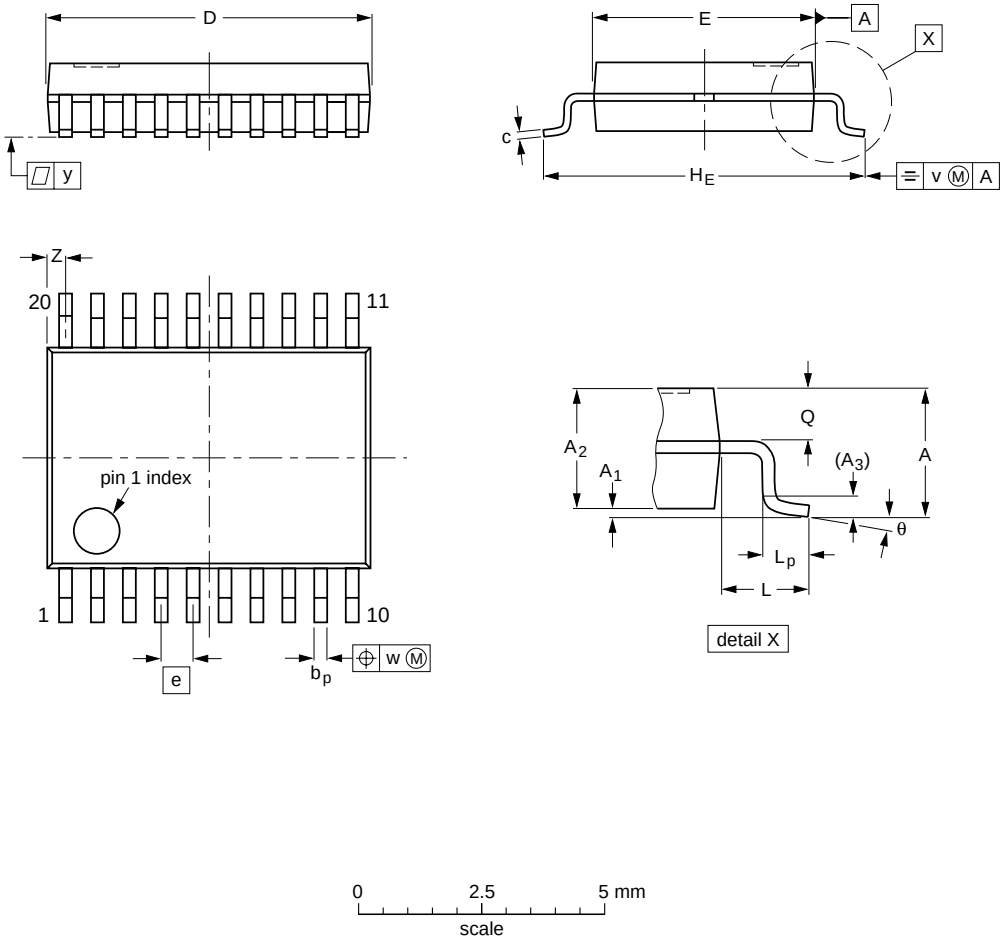
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~95-01-24~~ 97-05-22

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm **SOT266-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT266-1							~~90-04-05~~ 95-02-25

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO and SSOP

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO and SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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